
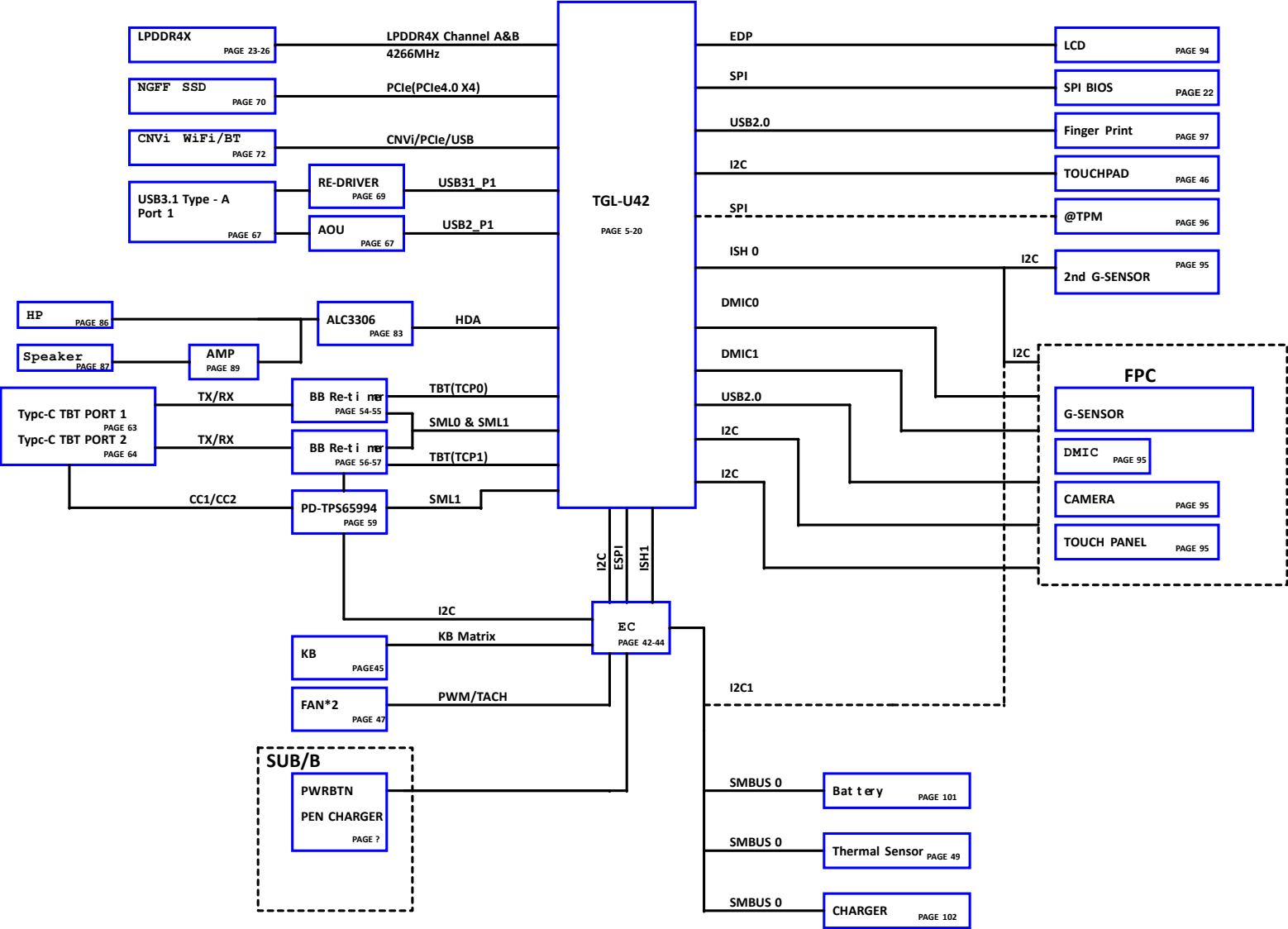


C950 Logic


Security Classification	LC Future Center Secret Data			Title				
Issued Date	2019/06/12	Deciphered Date	2020/06/12	TITLE PAGE				
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Date:				Thursday, August 13, 2020	Sheet	1	of	123

C950 TGL-U42 Schematic Block Diagram

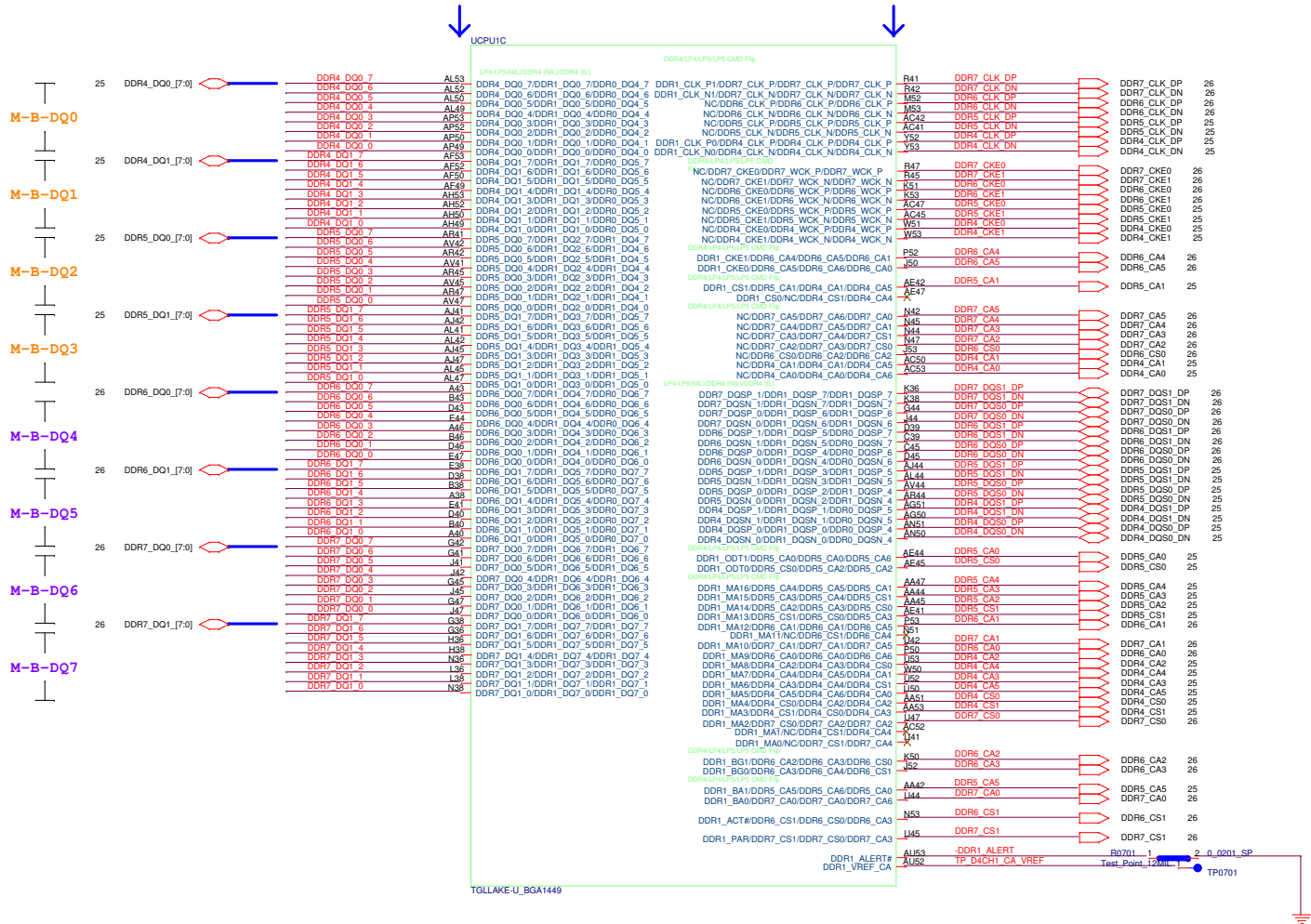


16,23,106,123 VCC1R1A  VCC1R1A



Title		
CPU(2/16): DDR1(1/2)		
Size C	Document Number	Rev
	C950	2.0

LPDDR4X CHANNEL 1



DBG_PMODE (DFx Test Mode)	
HIGH	DFx Test Mode Disabled (default) *
LOW	DFx Test Mode Enabled

GPP_F7 (Reserved) - Should Sample LOW	
HIGH	
LOW	(Default)

GPP_F10 (Reserved) - Should Sample LOW	
HIGH	
LOW	(Default)

GPP_C5/SML0ALERT# (Boot Strap Bit 0)	
GPP_H0 (Boot Strap Bit 1)	
GPP_H1 (Boot Strap Bit 2)	
GPP_H2 (Boot Strap Bit 3)	
0000b	Master Attached Flash Configuration (Default)

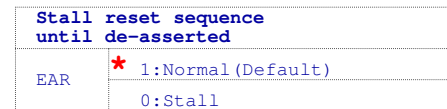


TABLE : Functional Strap

SPI0_MOSI (Boot Halt)		
HIGH	Disabled	★
LOW	Enabled	

TABLE : Functional Strap

SPI0_IO3 (A0 Personality Strap)		
HIGH	Disabled	★
LOW	Enabled	

TABLE : Functional Strap

GPP_C2/SMBALERT# (TLS Confidentiality)		
HIGH	Disable Flash Descriptor Security	
LOW	Enable Flash Descriptor Security	★

TABLE : Functional Strap

SPI0_IO2 (Consent Strap)		
HIGH	Disabled	★
LOW	Enabled	

TABLE : Functional Strap

GPP_E6 (JTAG ODT Disable)		
HIGH	JTAG ODT Enabled	★
LOW	JTAG ODT Disabled	

TABLE : Functional Strap

GPP_B23/SML1ALERT#/PCHHOT# (CPUNSSC Clock Frequency)		
HIGH	19.2MHz Clock (Derived from 38.4MHz Crystal)	
LOW	38.4MHz Clock (Direct from Crystal)	★

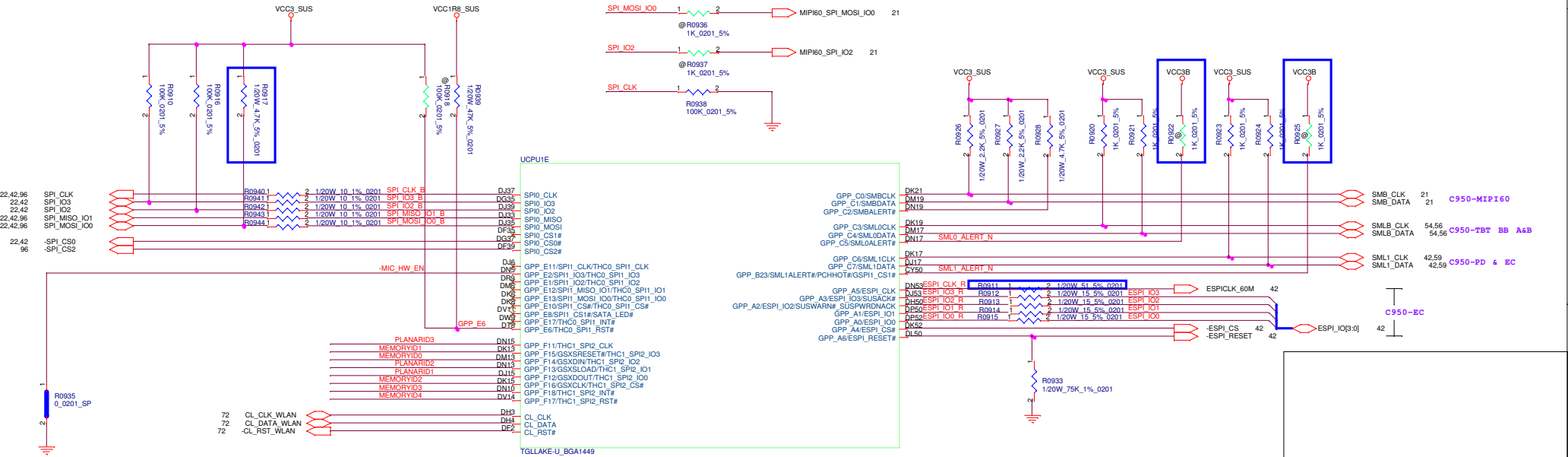
TABLE : Functional Strap

GPP_C5/SML0ALERT# (Boot Strap Bit 0)		
GPP_H0 (Boot Strap Bit 1)		
GPP_H1 (Boot Strap Bit 2)		
GPP_H2 (Boot Strap Bit 3)		
0000b	Master Attached Flash Configuration (Default)	

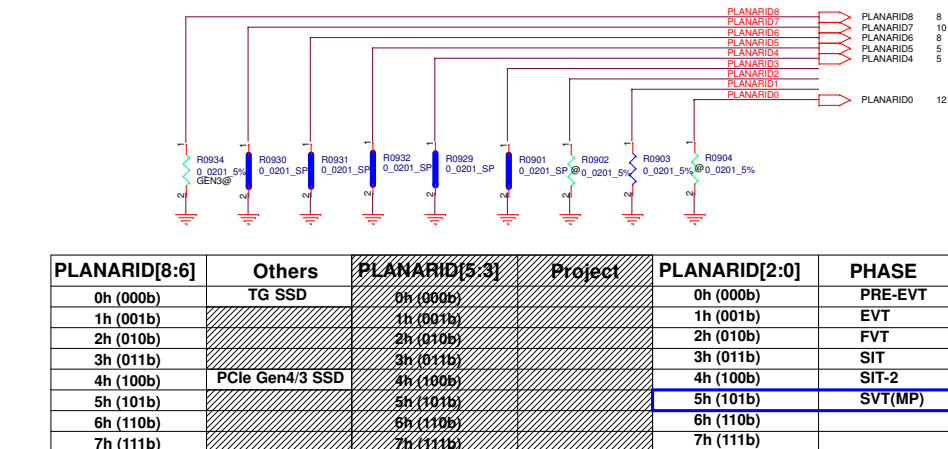
5,10,12,15,18,21,22,42,59,69,72,90,96,99,108,109

VCC3_SUS

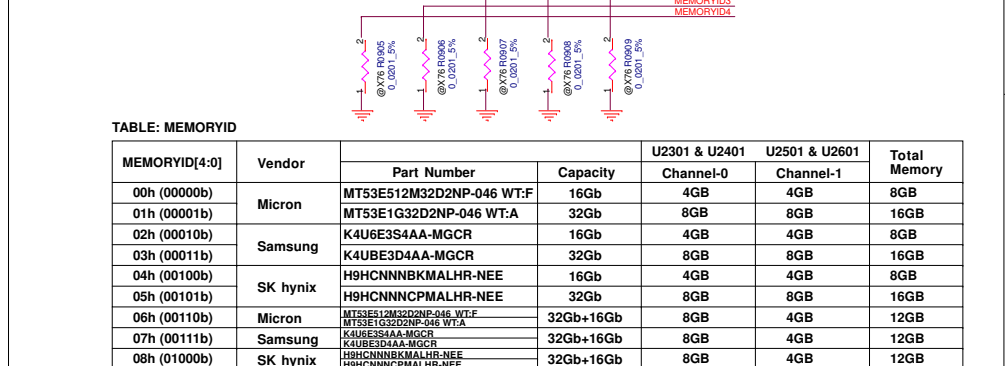
VCC3_SUS



PLANAR ID



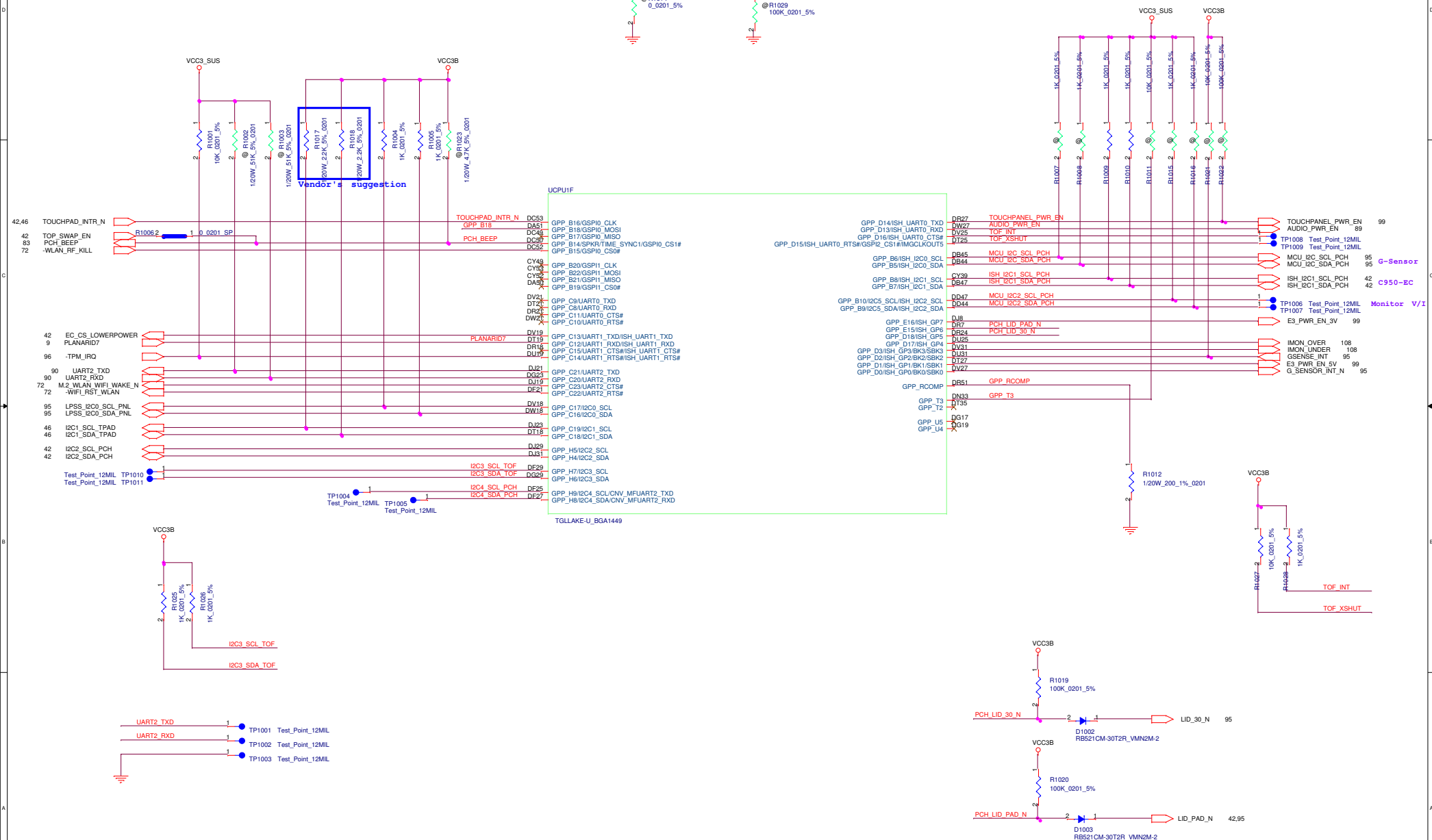
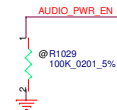
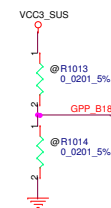
MEMORY ID



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Issued Date	2019/06/12	Deciphered Date	2020/06/12	CPU(5/16): SPI/ESPI/SMB/CL	
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GPP_B14/SPKR (Top Swap Override)	
HIGH	Enable "Top Swap" mode
LOW	Disable "Top Swap" mode (Default)★

GPP_B18/GSPI0_MOSI (No Reboot)	
HIGH	Enable "No Reboot" Mode
LOW	Disable "No Reboot" Mode (Default) ★




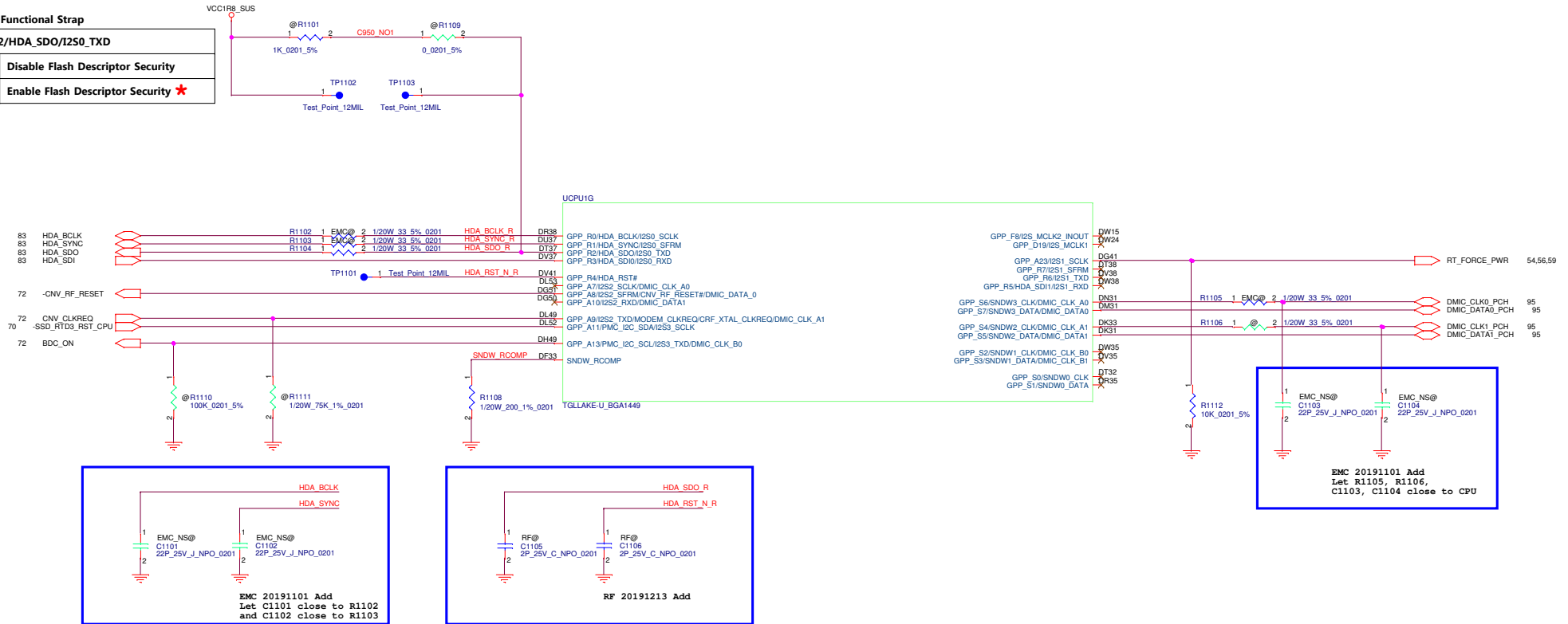
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Issued Date	2019/06/12	Deciphered Date	2020/06/12	CPU(6/16)-I2C/ISH/UART/GPIO		
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						C950
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TABLE : Functional Strap

GPP_R2/HDA_SDO/I2S0_TXD	
HIGH	Disable Flash Descriptor Security
LOW	Enable Flash Descriptor Security *




Security Classification	LC Future Center Secret Data			Title			
Issued Date	2019/06/12	Deciphered Date	2020/08/12	CPU(7/16): AUDIO			
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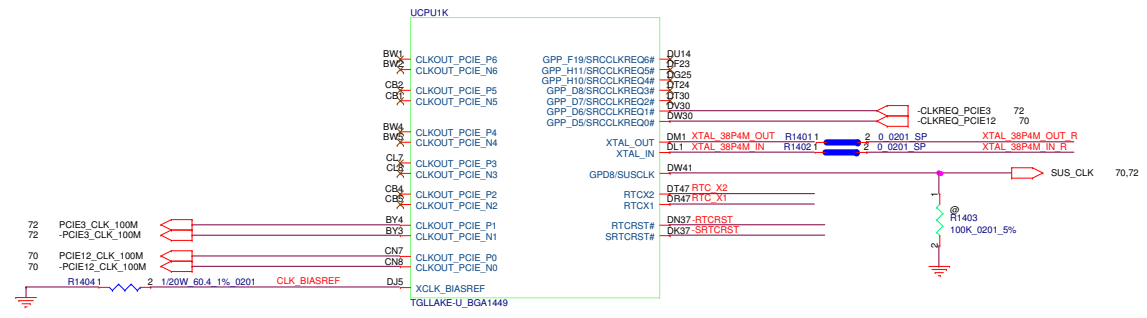
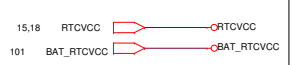
TABLE : Functional Strap

GPP_F2/CNV_RGI_DT(M.2 CNVi Mode Select)			
HIGH	Integrated	CNVi	Disabled
LOW	Integrated	CNVi	Enabled *

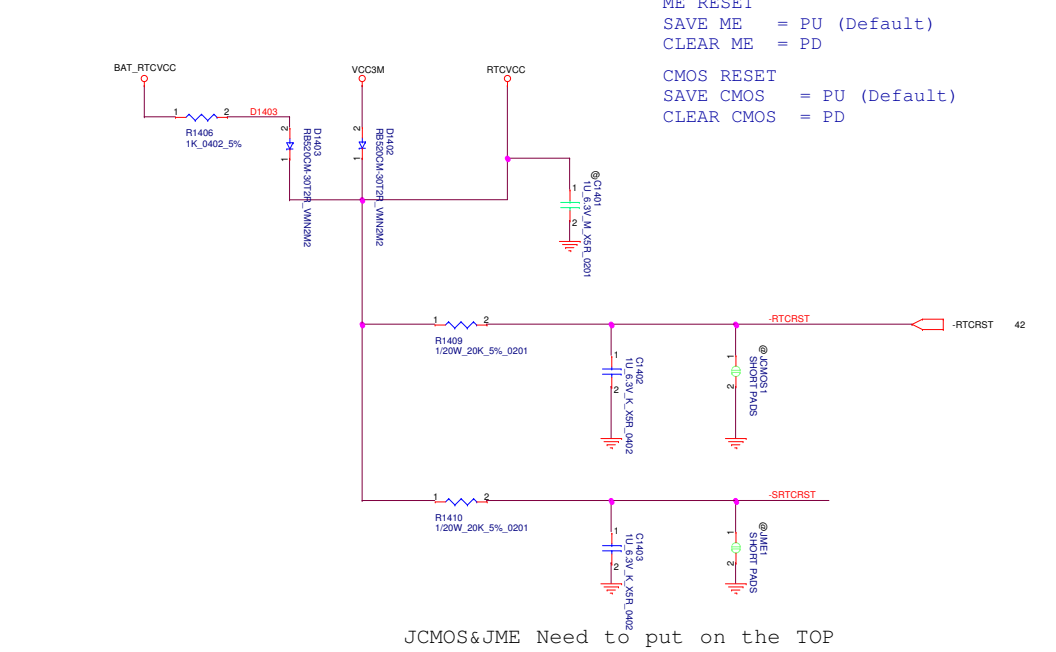
TABLE : Functional Strap

GPP_F0/CNV_BRI_DT (XTAL Frequency Selection)			
HIGH	24MHz	XTAL	selected
LOW	38.4MHz	XTAL	frequency selected *

PCIe CLK Table	
CLK 100M_P0	PCIe Gen3/4 SSD
CLK 100M_P1	M.2 Key-B WLAN
CLK 100M_P2	Reserved
CLK 100M_P3	Reserved
CLK 100M_P4	Reserved
CLK 100M_P5	Reserved
CLK 100M_P6	Reserved



RTC BATTERY



CRYSTAL - 32.768KHZ

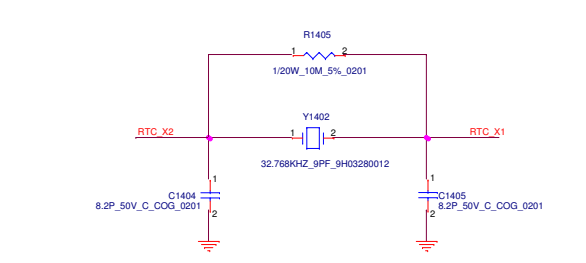


TABLE of Y1404		
Vendor	P/N	LCFC P/N
TXC	9H03280012	SJ10000J900
EPSON	X1A000141000201	SJ10000IX01
KDS	1TJF090DJ1A000B	SJ100069400

CRYSTAL - 38.4MHZ

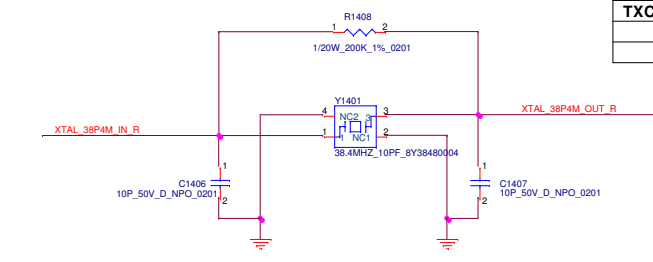
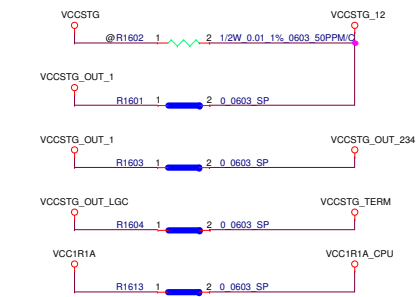


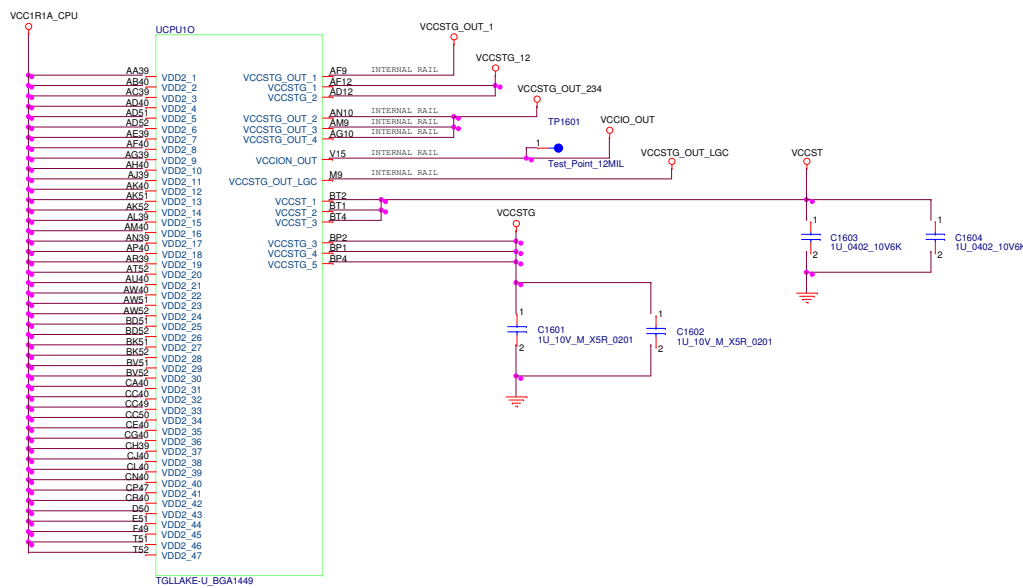
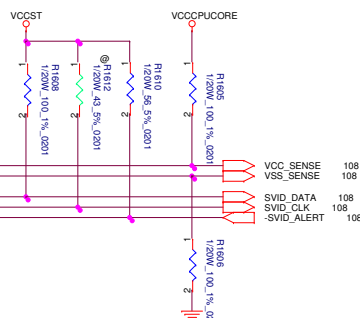
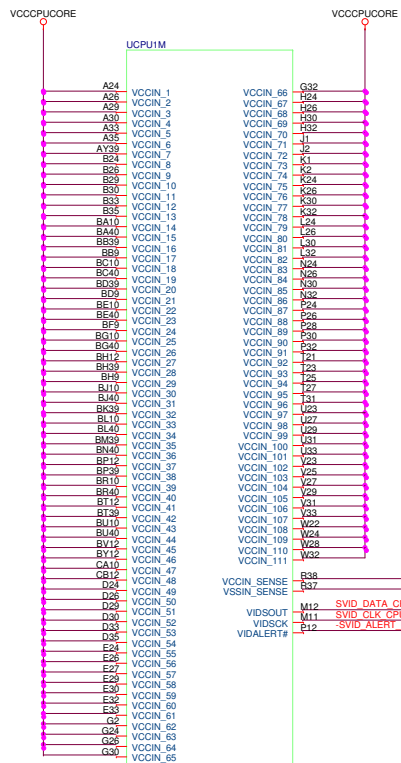
TABLE of Y1402		
Vendor	P/N	LCFC P/N
TXC	8Y38480004	SJ10000SN00

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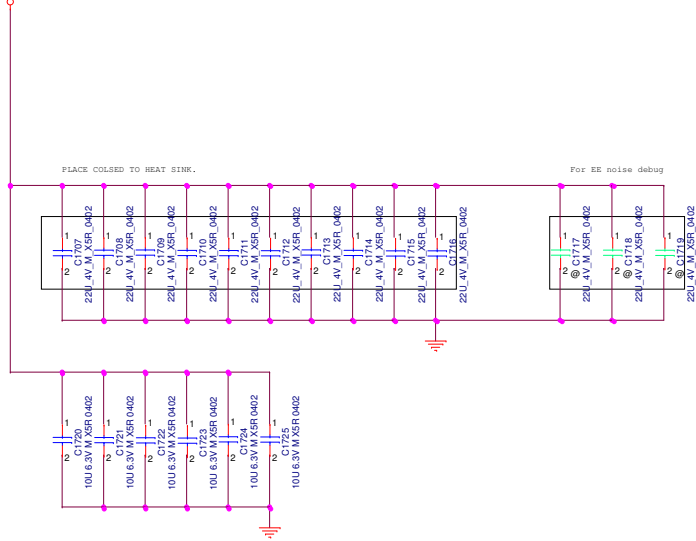
Current Sense Resistor	
R1601	10m
R1603	10m
R1604	10m
R1613	10m

17,108	VCCCPUCORE	VCCCPUCORE
	VCCSTG_12	VCCSTG_12
	VCCSTG_OUT_1	VCCSTG_OUT_1
	VCCSTG_OUT_234	VCCSTG_OUT_234
	VCCSTG_OUT_LGC	VCCSTG_OUT_LGC
8,15,42,99,108	VCCST	VCCST
23,106,123	VCC1R1A	VCC1R1A
8	VCCSTG_TERM	VCCSTG_TERM
8.99	VCCSTG	VCCSTG
20,21	VCCIO_OUT	VCCIO_OUT
6,17	VCC1R1A_CPU	VCC1R1A_CPU



VCCCPUCORE CAP

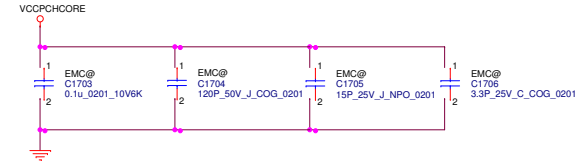
VCCCPUCORE



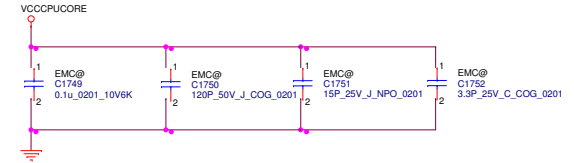
VCCCPUCORE	PDG	LCFC
330uF_B2 (CS)	2	HW:0/PWR:2
22uF_0603 (CS)	10	HW:0/PWR:0
10uF_0402 (CS)	29	HW:0/PWR:0
10uF_0402 (SS)	6	HW:0/PWR:0

Update on 2019/10/15
Follow 607872_TGL_UP3_PDG_Rev0p9

EMC



EMC CAPS -PLACEMENT: < 5MM FROM SOC'S VCCIN_AUX

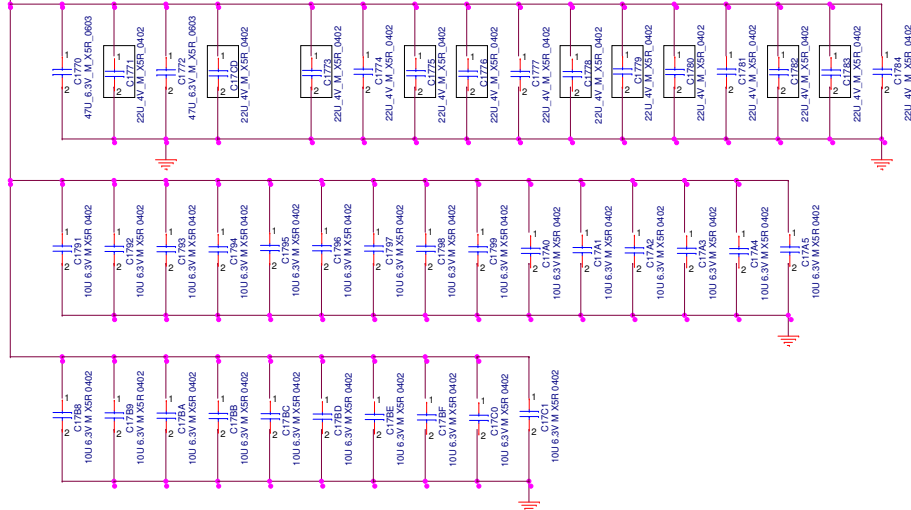


EMC CAPS -PLACEMENT: < 5MM FROM SOC'S VCCIN

VCCPCHCORE CAP

VCCPCHCORE

VCCPCHCORE	PDG	LCFC
220uF_B2 (CS)	1	HW:0/PWR:0
47uF_0603 (CS)	3	HW:0/PWR:0
22uF_0603 (CS)	12	HW:0/PWR:0
10uF_0402 (CS)	15	HW:0/PWR:0
10uF_0402 (SS)	10	HW:0/PWR:0

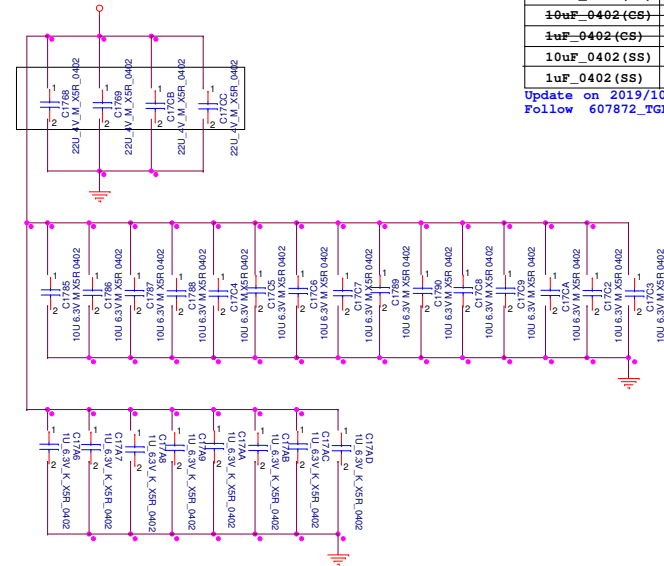


VCC1R1A_CPU CAP

VCC1R1A_CPU

VCC1R1A_CPU	PDG	LCFC
47uF_0603 (CS)	2	HW:0/PWR:0
10uF_0402 (CS)	4	HW:0/PWR:0
1uF_0402 (SS)	8	HW:0/PWR:0
10uF_0402 (SS)	13	HW:0/PWR:0
1uF_0402 (SS)	8	HW:0/PWR:0

Update on 2019/10/15
Follow 607872_TGL_UP3_PDG_Rev0p9



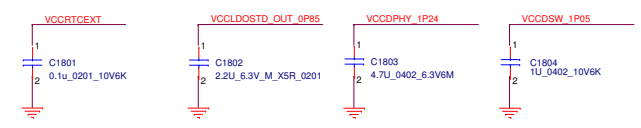
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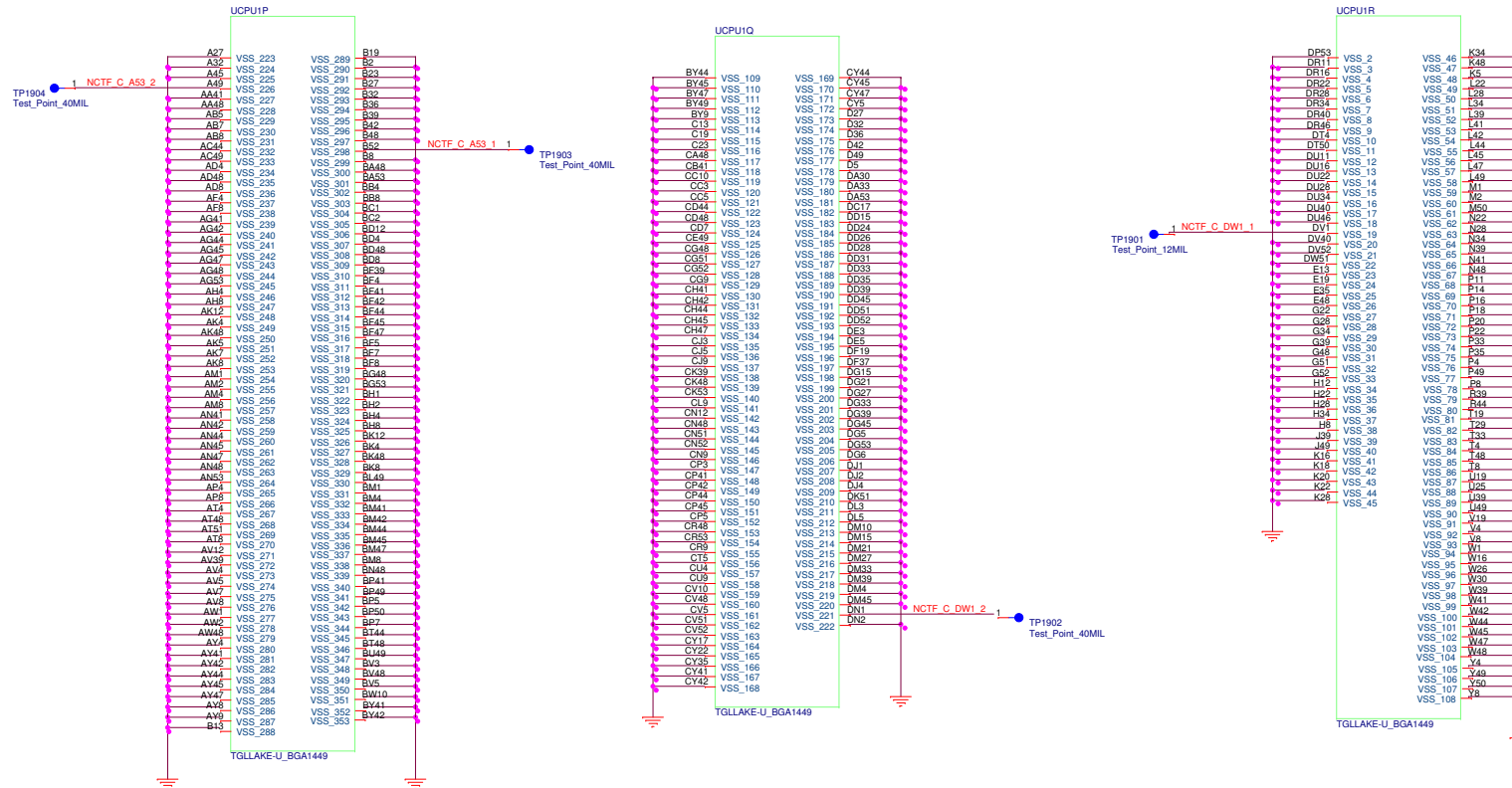


VID Table :

VID[1]	VID[0]	VCCPCHCORE
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

PCH POWER RAIL DE-COUPLING

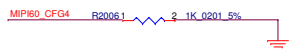




PROCESSOR CFG STRAPS

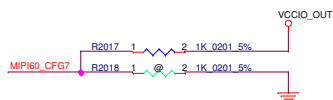
eDP Enable

CFG4 1:Disable
★ 0:Enable(Default)



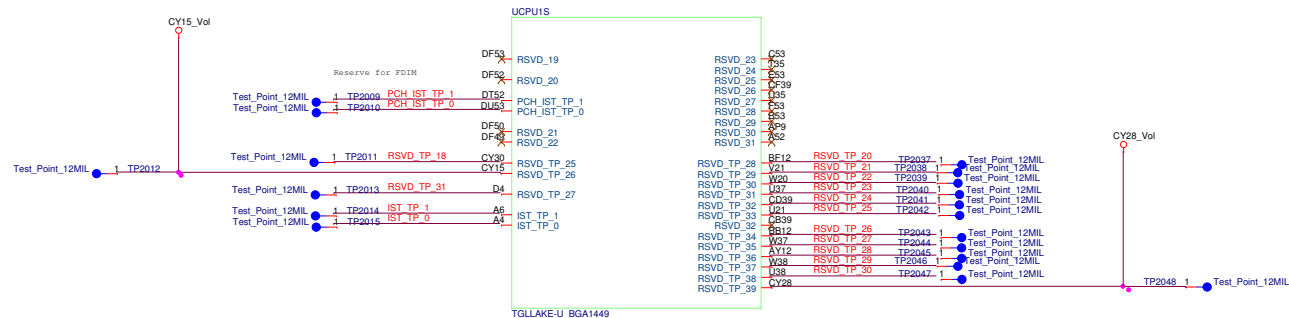
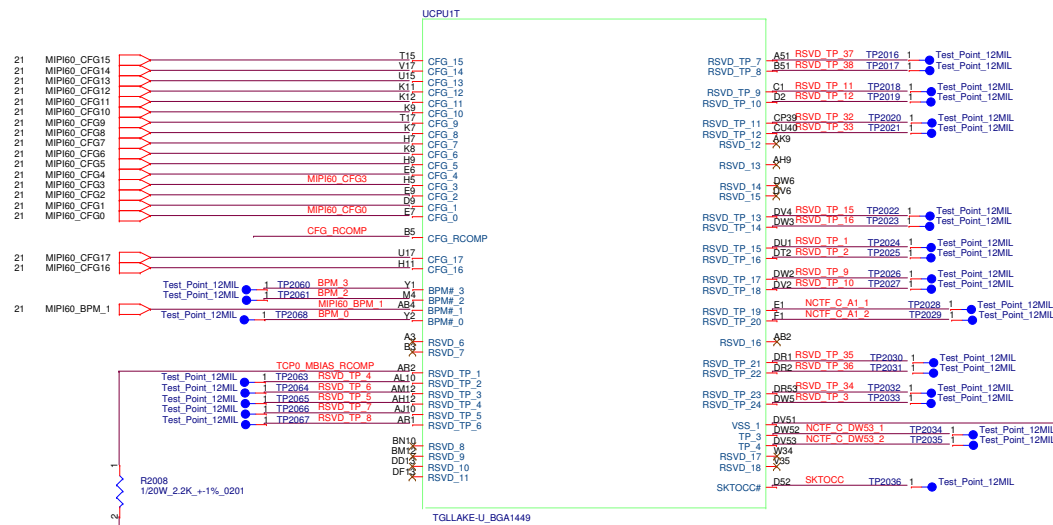
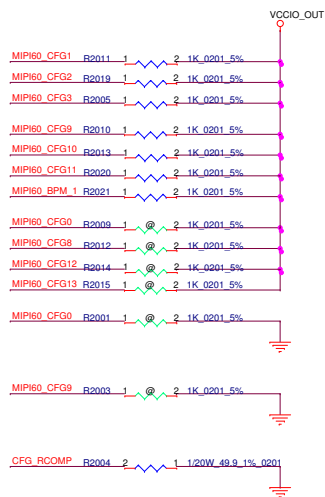
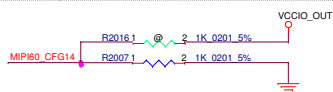
PEG Deferred Link Training

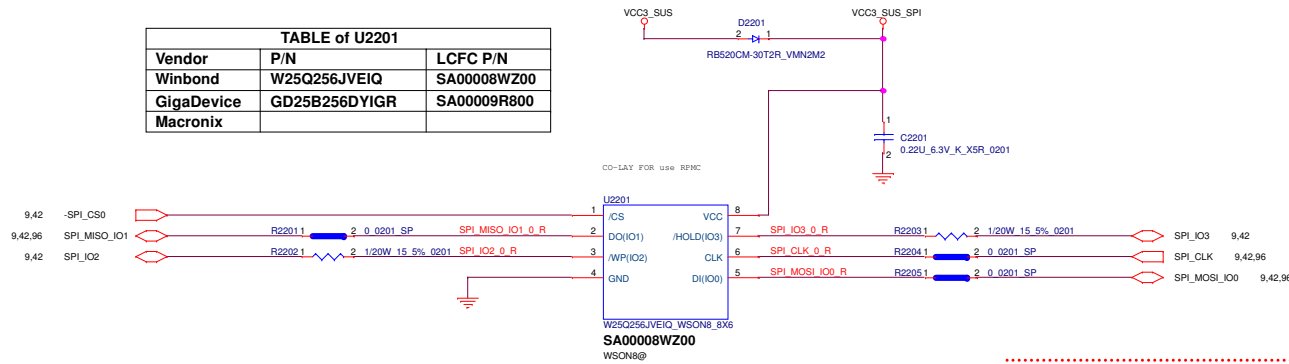
CFG7 ★ 1:Enabled
0:Disabled



PEG60 Lane Reversal

CFG14 1:Reversal (Default)
★ 0:Reserved





SF100 PIN HEADER INTERFACE (TOP VIEW)					
1	VCC	D0901.1	GND	GND	2
3	CS#	U2201.1	R2204.1	CLK	4
5	MISO	R2201.1	R2205.1	MOSI	6
7	(KEY)	N/A	N/A	(RESET)	8

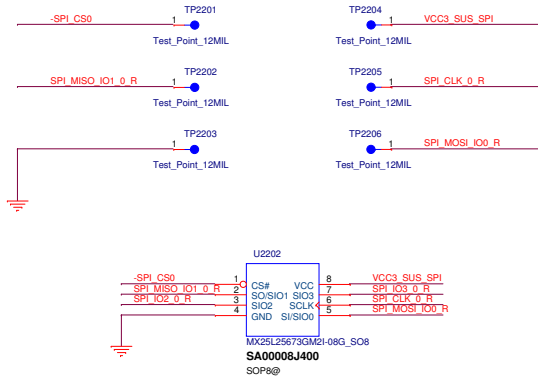
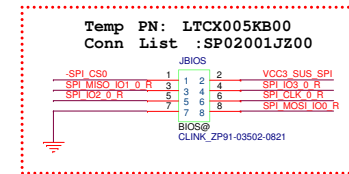
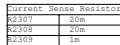
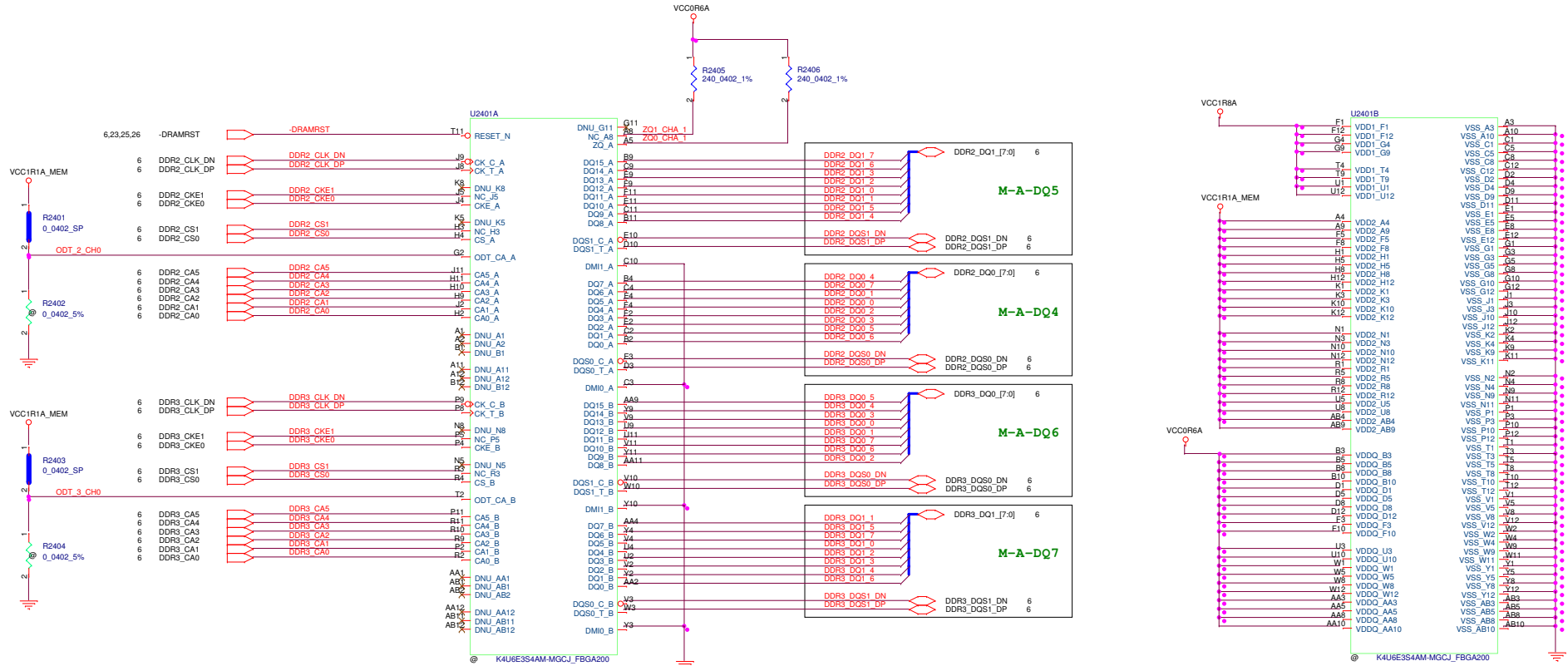


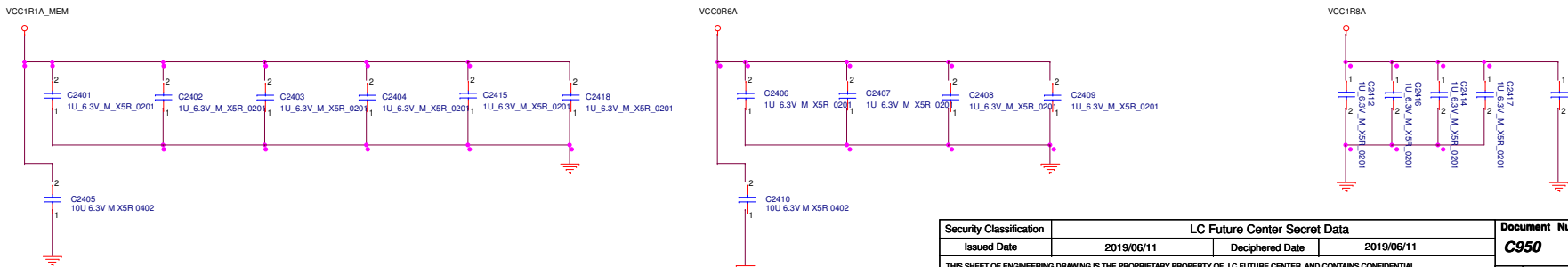
TABLE of U2202		
Vendor	P/N	LCFC P/N
Macronix	MX25L25673GM2I-08G	SA00008J400
GigaDevice	W25Q256JVEIQ	SA00008WZ00
Winbond	GD25B256DYIGR	SA00009R800

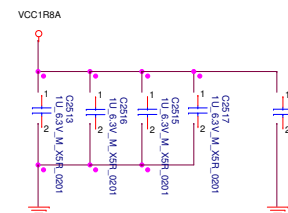
LCFO

Rev



23,25,26 VCC1R8A
23,25,26 VCC0R6A
23,25,26 VCC1R1A_MEM






LCFC

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Size	Title	Rev								
C	LPDDR4X CHANNEL.....	2.0								
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Size C	Title GPU (1/8) : PEQ I/F	Date: Thursday, August 13, 2020			Rev 2.0
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Security Classification	LC Future Center Secret Data			Document Number	LCFC
Issued Date	2019/06/11	Deciphered Date	2019/06/11	<i>C950</i>	
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Size C	Title GPU (2/8) : VRAM 1F			Rev 2.0	
Date: Thursday, August 13, 2020				Sheet	32 of 123


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Issued Date	2019/06/11	Deciphered Date	2019/06/11	C950	
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Size	C	Title	GPU (3/6) : POWER 1		Rev
		Date: Thursday, August 13, 2020		Sheet	33 of 123

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Security Classification	LC Future Center Secret Data			Document Number							
Issued Date	2019/06/11	Deciphered Date	2019/06/11	C950							
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Size	Title	Rev									
C	GPU (4/6) : POWER 2	2.0									
Date: Thursday, August 13, 2020					Sheet 34 of 123						

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Size	C	Title	GPU (5/6) : GND			Rev	2.0	
Date:		Thursday, August 13, 2020		Sheet		35	of	123

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Size	C	Title	VRAM CHANNEL-A		Rev
		Date: Thursday, August 13, 2020		Sheet	37 of 123

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Issued Date	2019/06/11	Deciphered Date	2019/06/11	<i>C950</i>	
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				Date: Thursday, August 13, 2020	Rev 2.0
				Sheet 38 of 123	

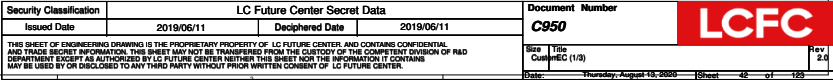
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Issued Date	2019/06/11	Deciphered Date	2019/06/11	C950	
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Size	C	Title	Load SW VIDEO		Rev
Date:		Thursday, August 13, 2020		Sheet	40 of 123
					2.0

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Security Classification	LC Future Center Secret Data			Document Number	LCFC		
Issued Date	2019/06/11	Deciphered Date	2019/06/11	MXM conn (For EC)			
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Date:					Thursday, August 13, 2020	Sheet	41 of 123



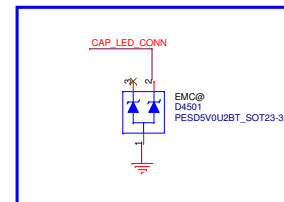
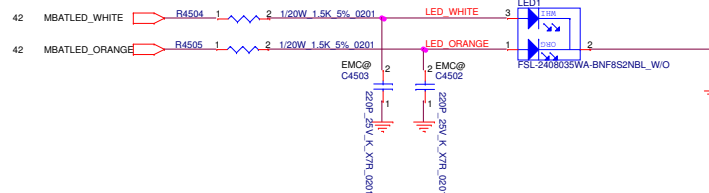
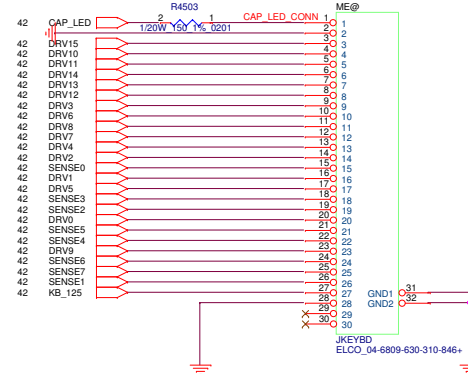
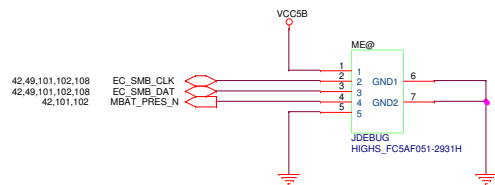
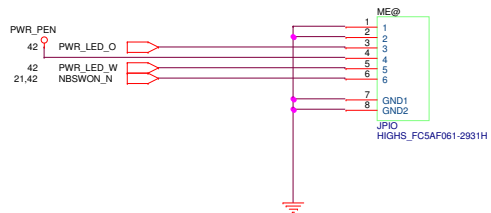
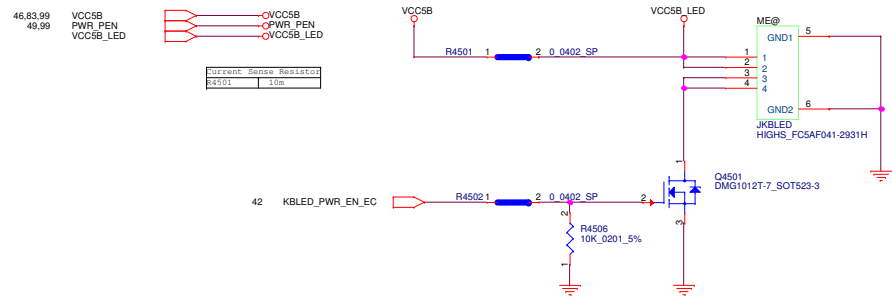
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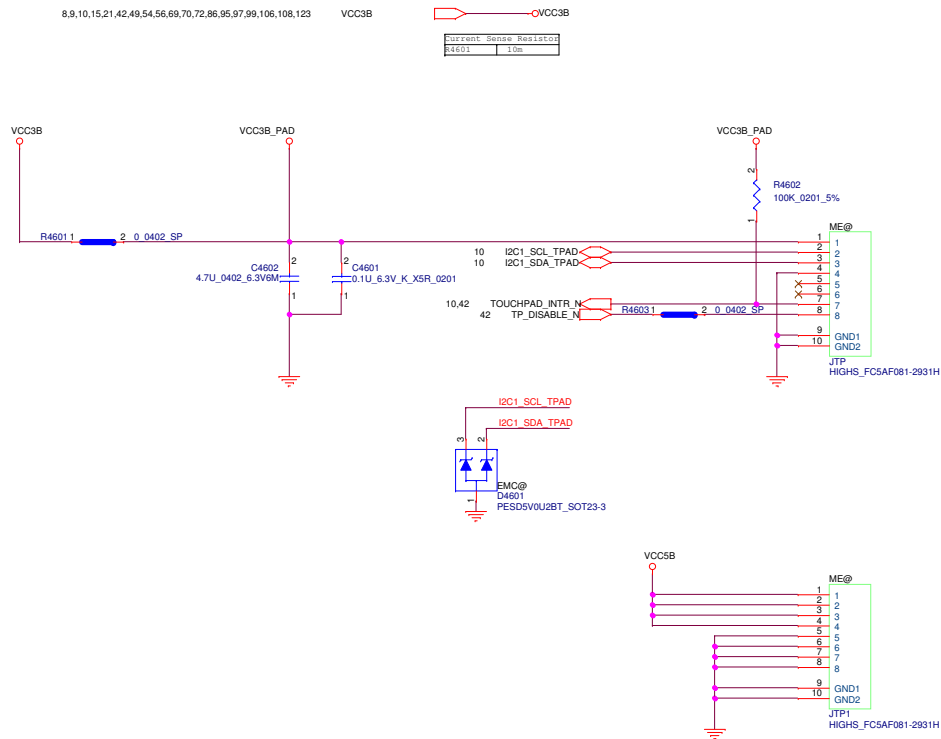
Security Classification		LC Future Center Secret Data		Document Number	
Issued Date	2019/06/11	Deciphered Date	2019/06/11	C950	
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				Title	2.0
Cust				wEC (2/3)	
Date:				Thursday, August 19, 2020	Sheet 43 of 123

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Size	Title	EC (3/3)			Rev
Custom					2.0
Date:		Thursday, August 13, 2020		Sheet	44 of 123

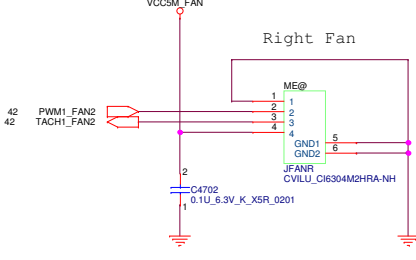
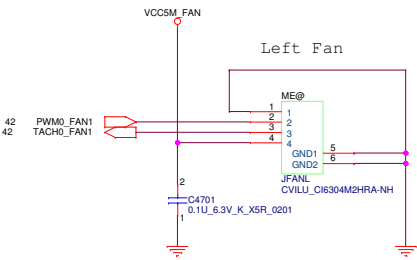
LCFC





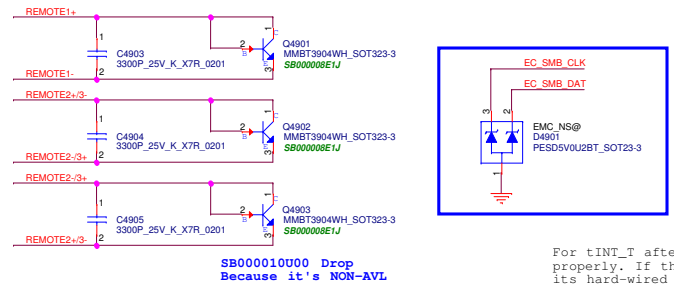
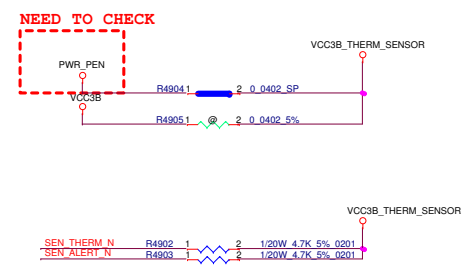
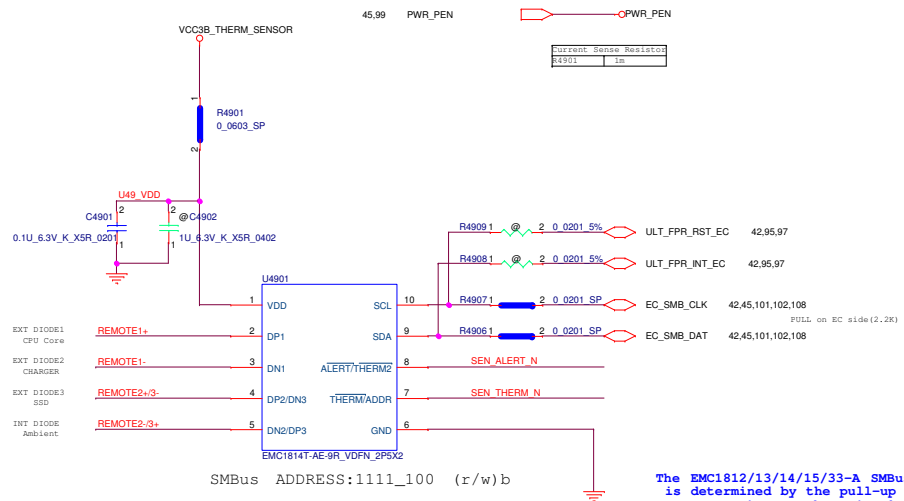
99 55,59,67,69,90,99,103,116,123
8,9,10,15,21,42,46,49,54,56,69,70,72,86,95,97,99,106,108,123

VCC5M_FAN
VCC5M
VCC3B



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Security Classification	LC Future Center Secret Data			Document Number	<div>LCFC</div>	
Issued Date	2019/06/11	Deciphered Date	2019/06/11	APS		
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Date:				Thursday, August 13, 2020	Sheet	48 of 123



The EMC1812/13/14/15/33-A SMBus slave address is determined by the pull-up resistor on the THERMADDR pin, as shown in the following table.

Pull-Up Resistor on THERM pin ($\pm 5\%$)	SMBus Address
4.7 k Ω	1111_100 (r/w)b
6.8 k Ω	1011_100 (r/w)b
10 k Ω	1001_100 (r/w)b
15 k Ω	1101_100 (r/w)b
22 k Ω	0011_100 (r/w)b
33 k Ω	0111_100 (r/w)b

For tINT_T after power-up, the THERM pin must not be pulled low or the I2C address will not be decoded properly. If the system requirements do not permit these conditions, the THERM pin must be isolated from its hard-wired OR'd bus during this time.

Please refer to EMC1814 spec page.34

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Date:					Thursday, August 13, 2020	Sheet 50 of 123

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Issued Date	2019/06/11	Deciphered Date	2019/06/11	C950	
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					Cuajm#Hink Engine (2/2) 2.0
					Date: Thursday, August 13, 2020 Sheet 51 of 123

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2019/06/11		2019/06/11		LCFC	
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Size	Document Number				Rev
Quoted	C950				2.0
Date:	Thursday, August 13, 2020		Sheet	59	of 129

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Issued Date	2019/06/11	Deciphered Date	2019/06/11	BLANK	
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Size	Document Number		Rev		
Date:	Thursday, August 13, 2020		Sheet 53 of 123		

VCC3B 8,9,10,15,21,42,46,49,56,69,70,72,86,95,97,99,106,108,123

VCC3M 14,15,18,42,55,59,70,72,95,99,102,105,106,108,109,116

VCC3P3_SX_TBTB 55

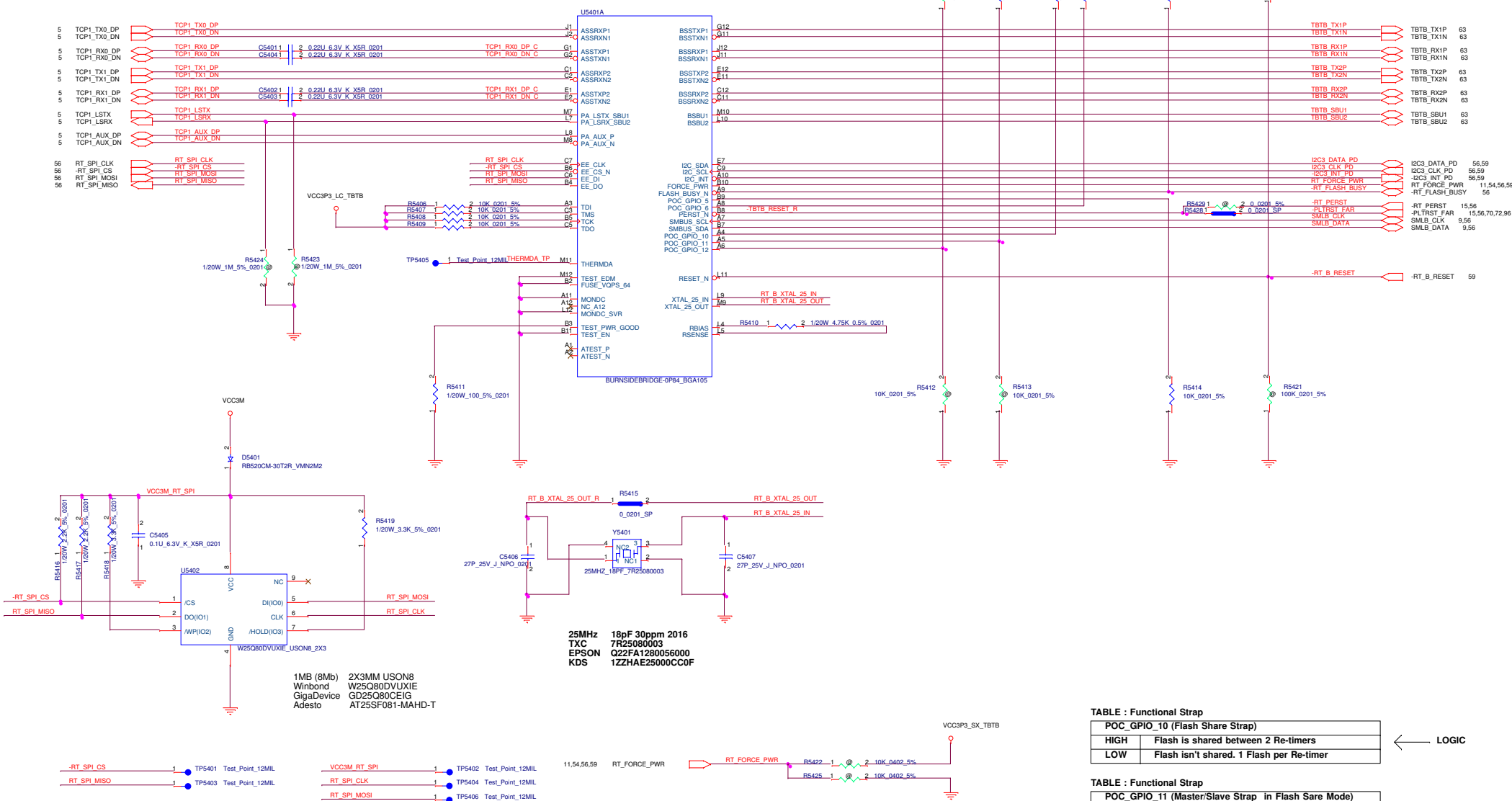


TABLE : Functional Strap

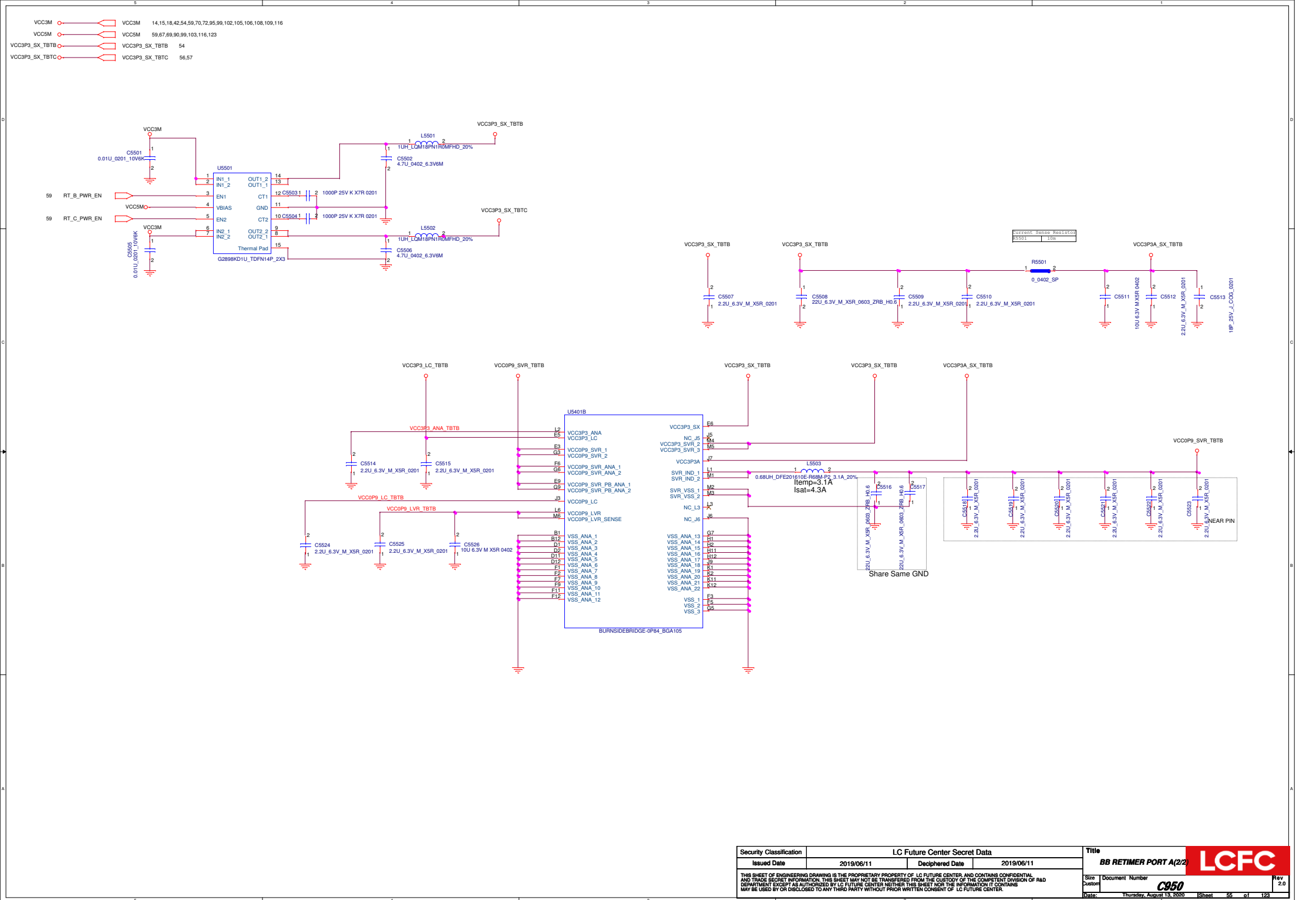
POC_GPIO_10 (Flash Share Strap)	
HIGH	Flash is shared between 2 Re-timers
LOW	Flash isn't shared. 1 Flash per Re-timer

← LOGIC

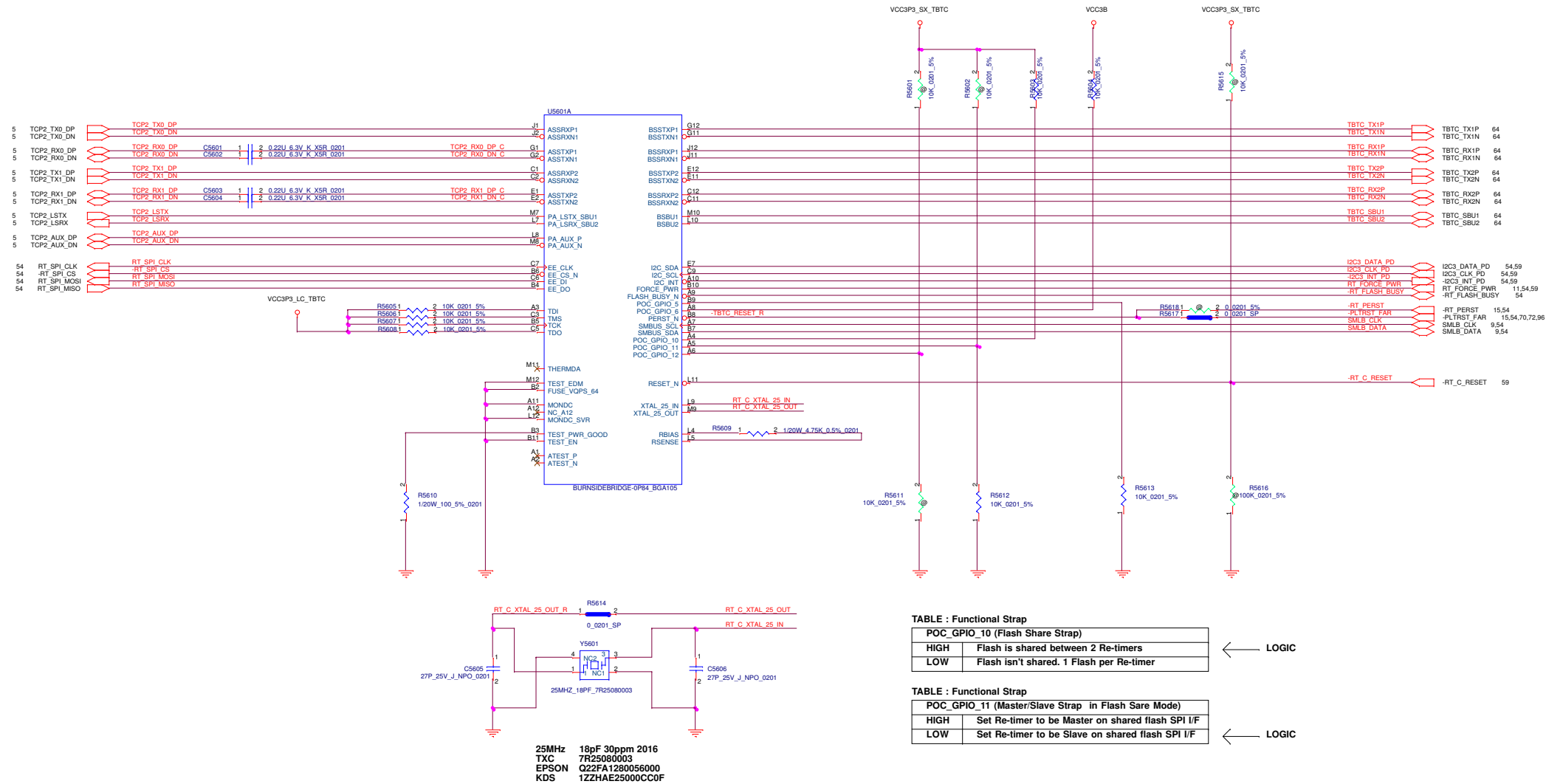
TABLE : Functional Strap

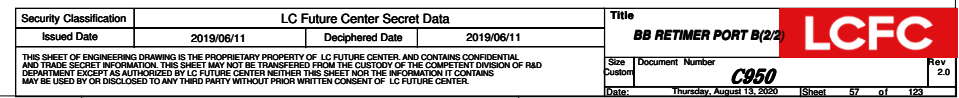
POC_GPIO_11 (Master/Slave Strap in Flash Sare Mode)	
HIGH	Set Re-timer to be Master on shared flash SPI I/F
LOW	Set Re-timer to be Slave on shared flash SPI I/F

← LOGIC



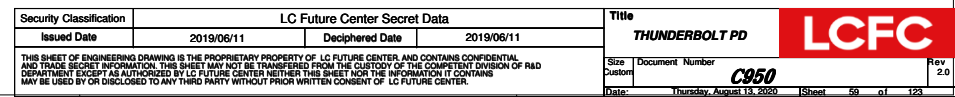
VCC3B 8,9,10,15,21,42,46,49,54,69,70,72,86,95,97,99,106,108,123
VCC3M 14,15,18,42,54,55,59,70,72,95,99,102,105,106,108,109,116
VCC3P3_SX_TBTC 55,57





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Quoted	C950	2.0			
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Size	Document Number	Rev			
Quoted	C950	2.0			
Date:	Thursday, August 13, 2020		Sheet	60	of 123

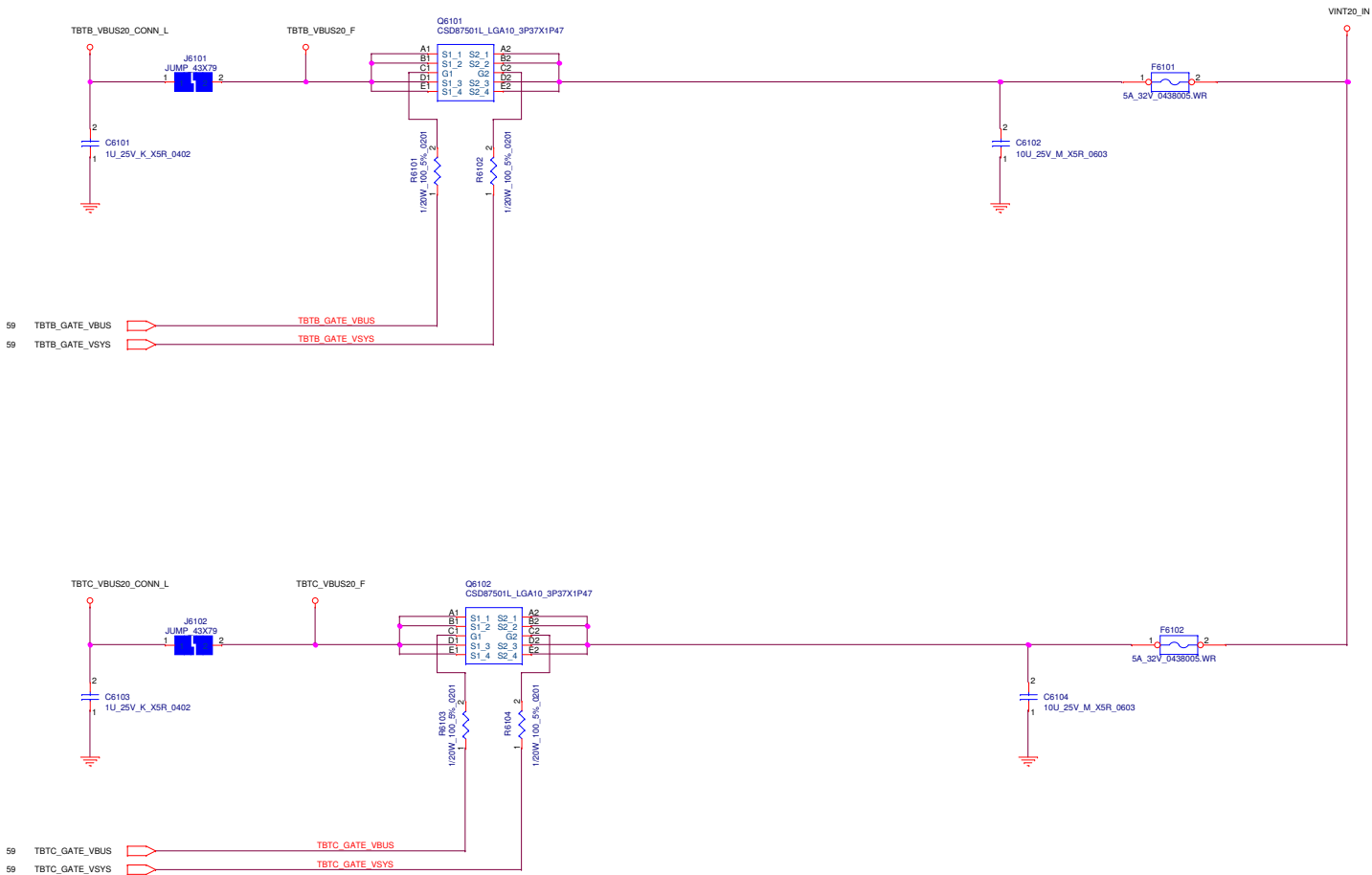
VINT20_IN 59.102

TBTB_VBUS20_CONN_L 59.63

TBTC_VBUS20_CONN_L 59.64

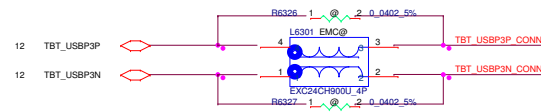
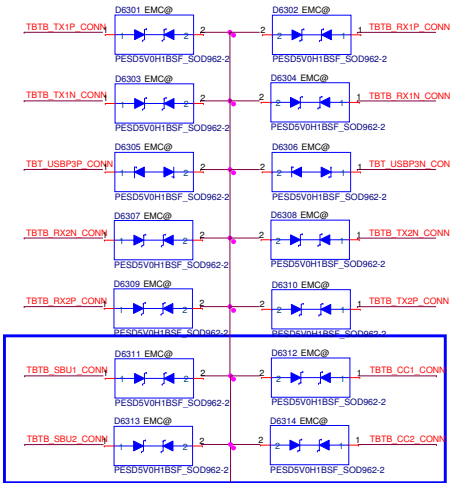
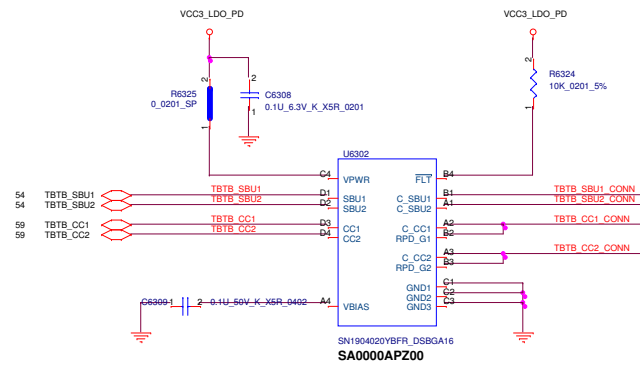
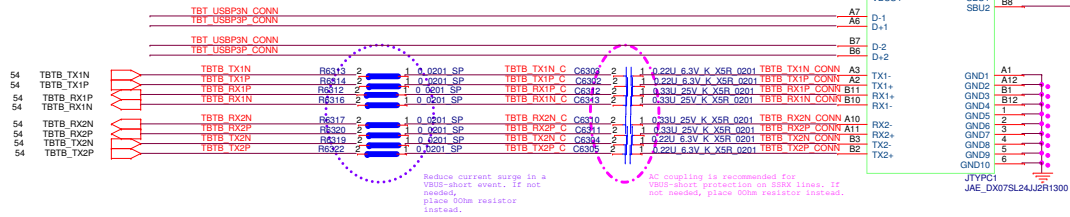
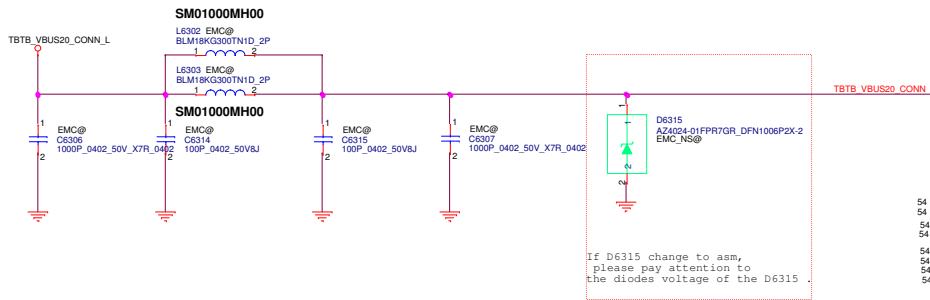
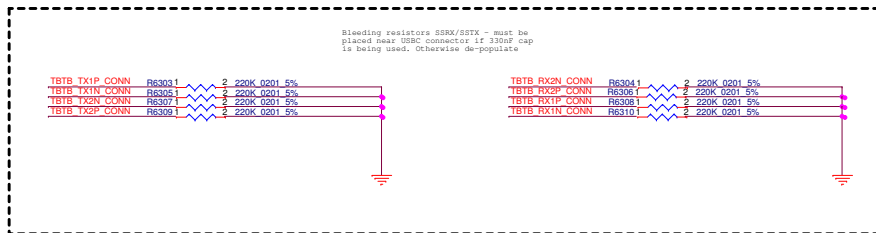
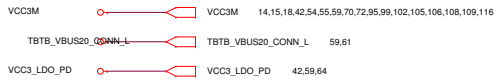
TBTB_VBUS20_F 59.64

TBTC_VBUS20_F 59.64



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Security Classification		LC Future Center Secret Data		Title	
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Size	Document Number	Rev			
Quoted	C950	2.0			
Date:	Thursday, August 13, 2020		Sheet	68	of 123

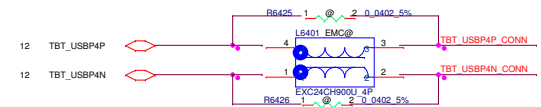
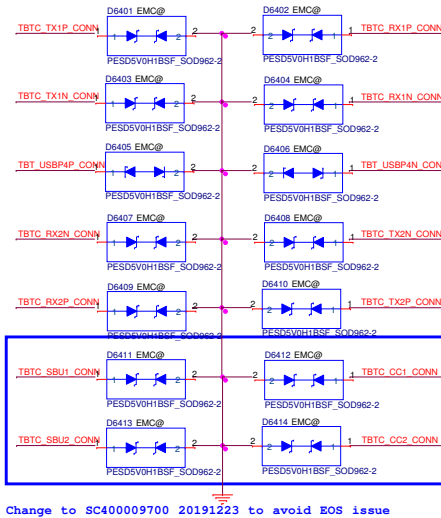
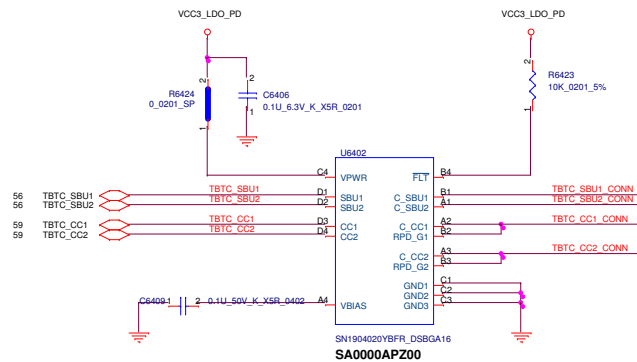
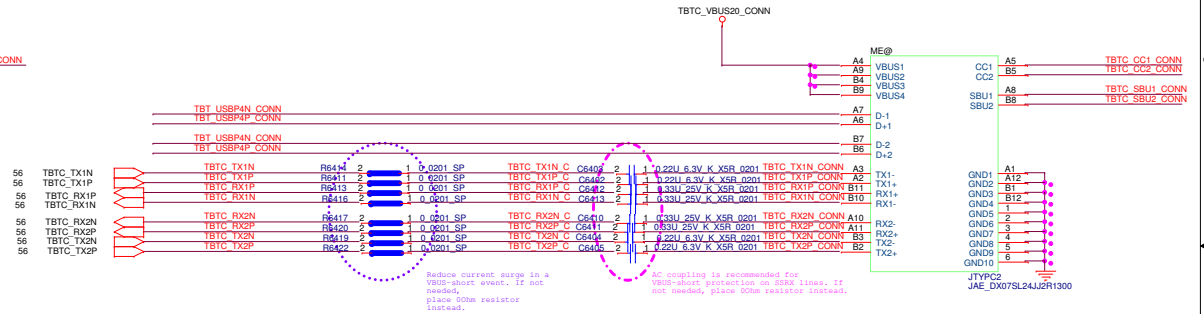
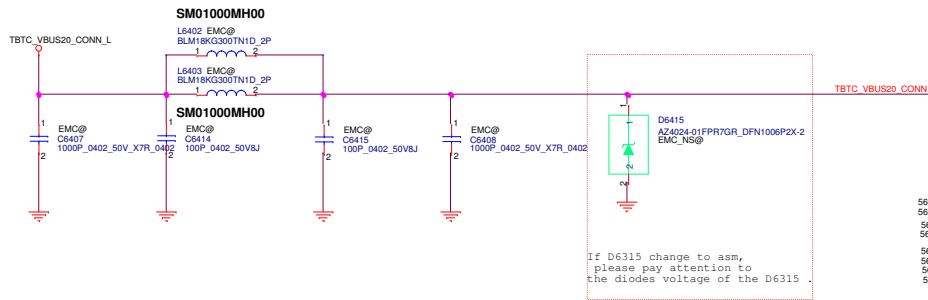
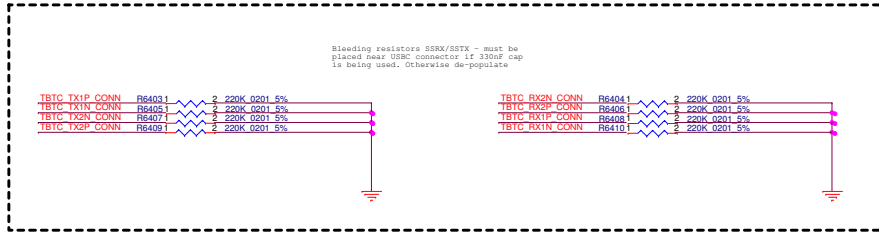


Change to SC400009700 20191223 to avoid EOS issue

VCC3M 14,15,18,42,54,55,59,70,72,95,99,102,105,106,108,109,116

TBTC_VBUS20_CONN_L 59,61

VCC3_LDO_PD 42,59,63



Security Classification	LC Future Center Secret Data		Title	
Issued Date	2019/06/11	Deciphered Date	2019/06/11	TBTC PORT B CONNECTOR
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Size	Document Number	Rev		2.0
Date	Thursday, August 13, 2020	Sheet	64 of 123	

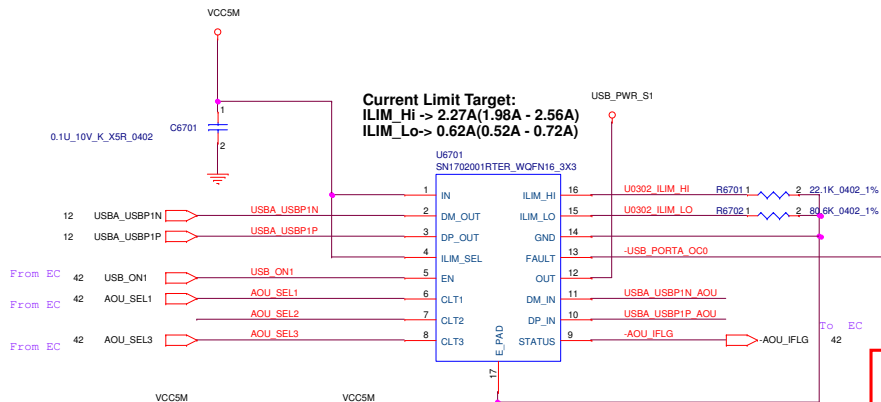
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Security Classification		LC Future Center Secret Data		Title	
Issued Date		Deciphered Date		CONN_T8T	
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Size	Document Number	C950			Rev
Quoted					2.0
Date:		Thursday, August 13, 2020		Sheet	65 of 123



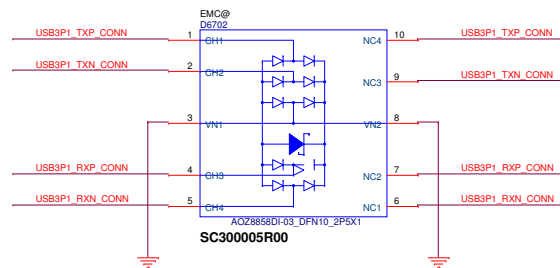
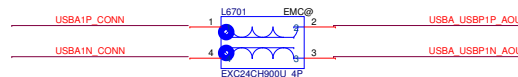
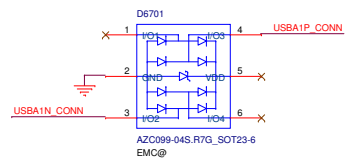
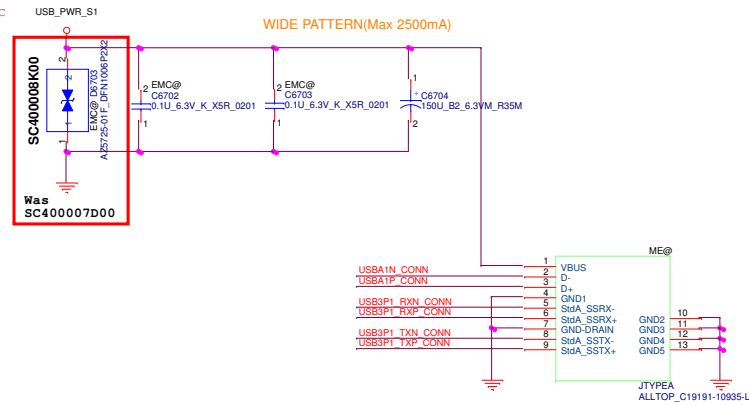
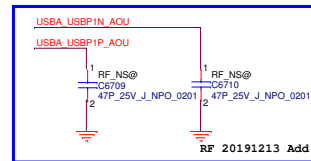
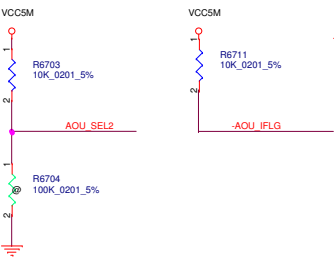
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2019/06/11		2019/06/11		LCFC	
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Size	Document Number	Rev			
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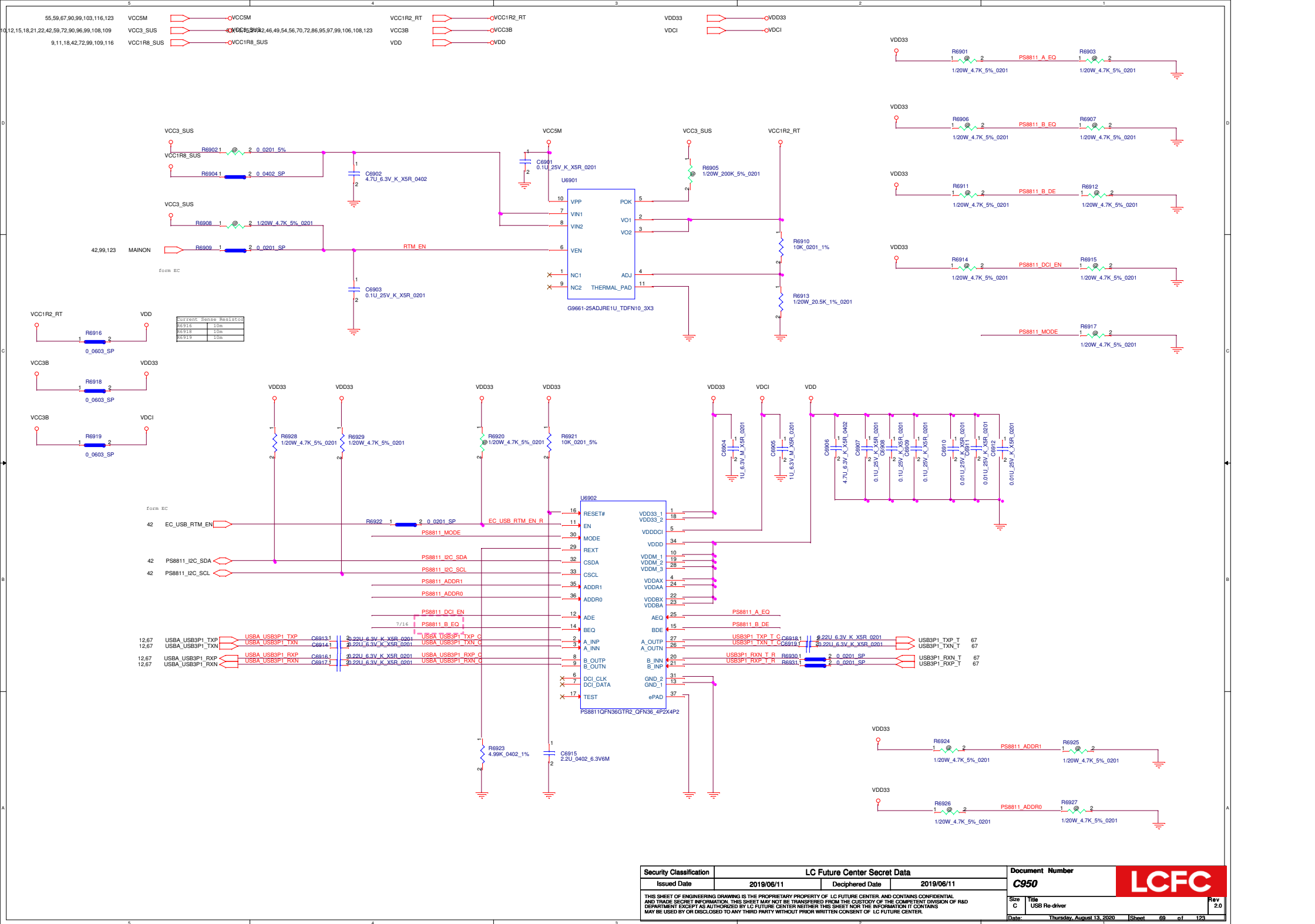
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12.69	USBA_USB3P1_TXN	USBA_USB3P1_TXN	R6706 1	DC0	2	0	0201 5%	USBA_USB3P1_TXN_R	DC0	C6706 1	2	0.22U 6.3V K XSR_0201	USB3P1_TXN_T
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12.69	USBA_USB3P1_RXN	USBA_USB3P1_RXN	R6708 1	DC0	2	0	0201 5%	USBA_USB3P1_RXN_R	DC0	C6708 1	2	0.22U 6.3V K XSR_0201	USB3P1_RXN_T

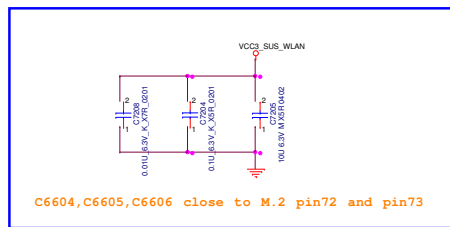
Colay for DCI



USB3P1_RXP_CONN	R6712 1	2	0	0402 SP	USB3P1_RXP_T	USB3P1_RXP_T	69
USB3P1_RXN_CONN	R6713 1	2	0	0402 SP	USB3P1_RXN_T	USB3P1_RXN_T	69
USB3P1_TXP_CONN	R6714 1	2	0	0402 SP	USB3P1_TXP_T	USB3P1_TXP_T	69
USB3P1_TXN_CONN	R6715 1	2	0	0402 SP	USB3P1_TXN_T	USB3P1_TXN_T	69

Change CMC to shortpad for MP





TABLE

TABLEVCC3 SUS WLAN

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Issued Date	2019/06/11	Deciphered Date	2019/06/11	
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Generated: 2019-06-11 15:00:00			2019-06-11 15:00:00	128

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Size	Title	Rev								
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<small>Date:</small>				<small>Thursday, August 13, 2020</small>		
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Rev				2.0	

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Issued Date	2019/06/11	Deciphered Date	2019/06/11	C950			
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Date:				Thursday, August 13, 2020		
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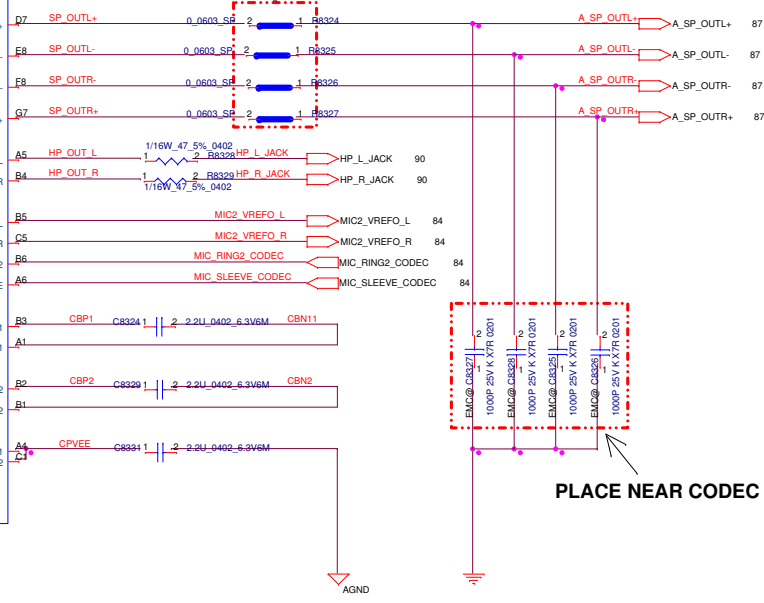
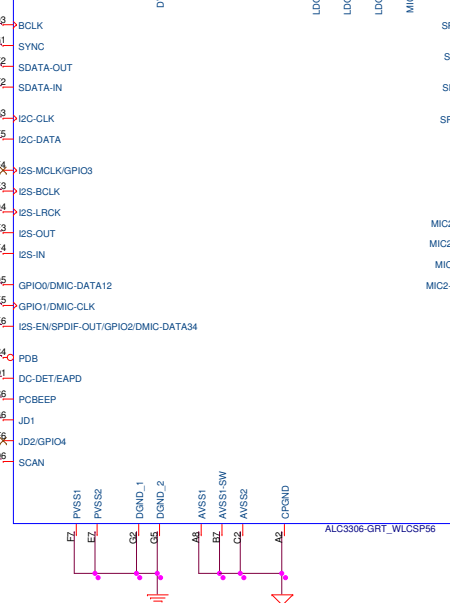
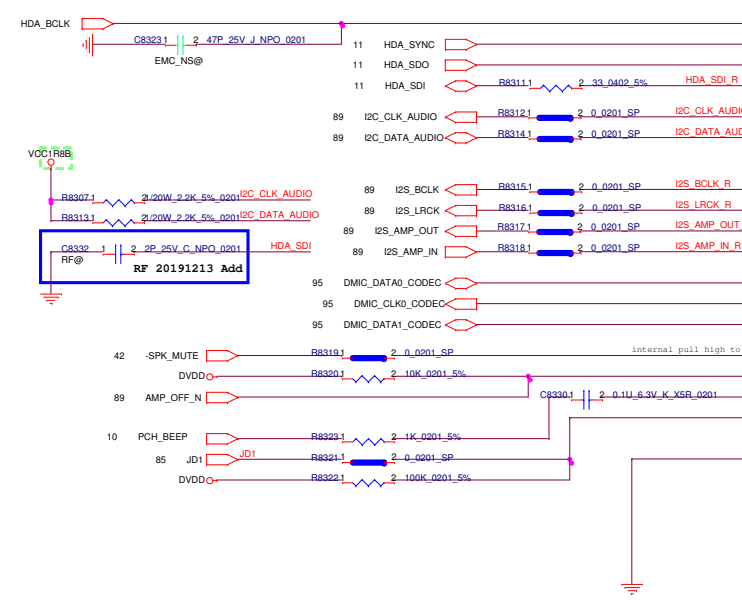
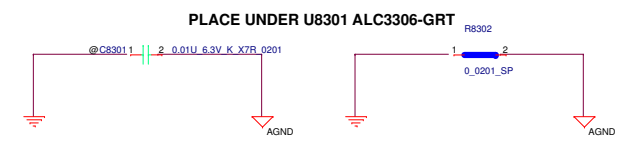
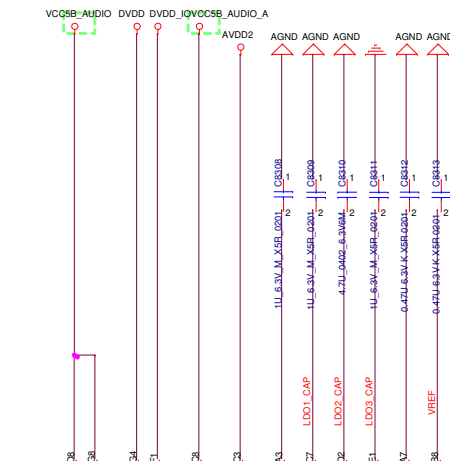
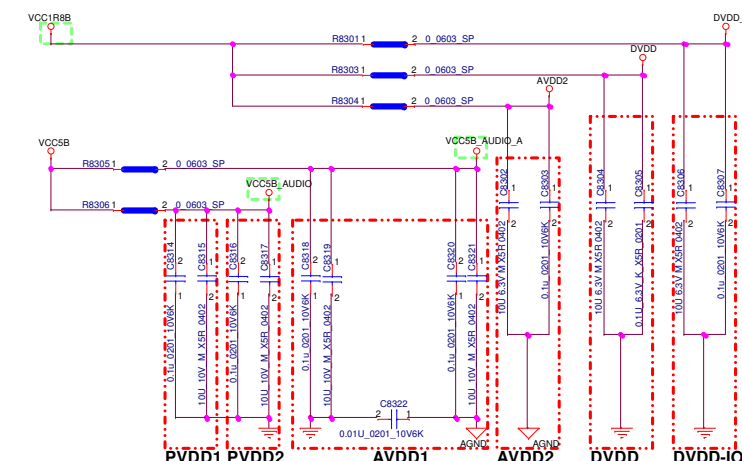
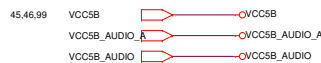
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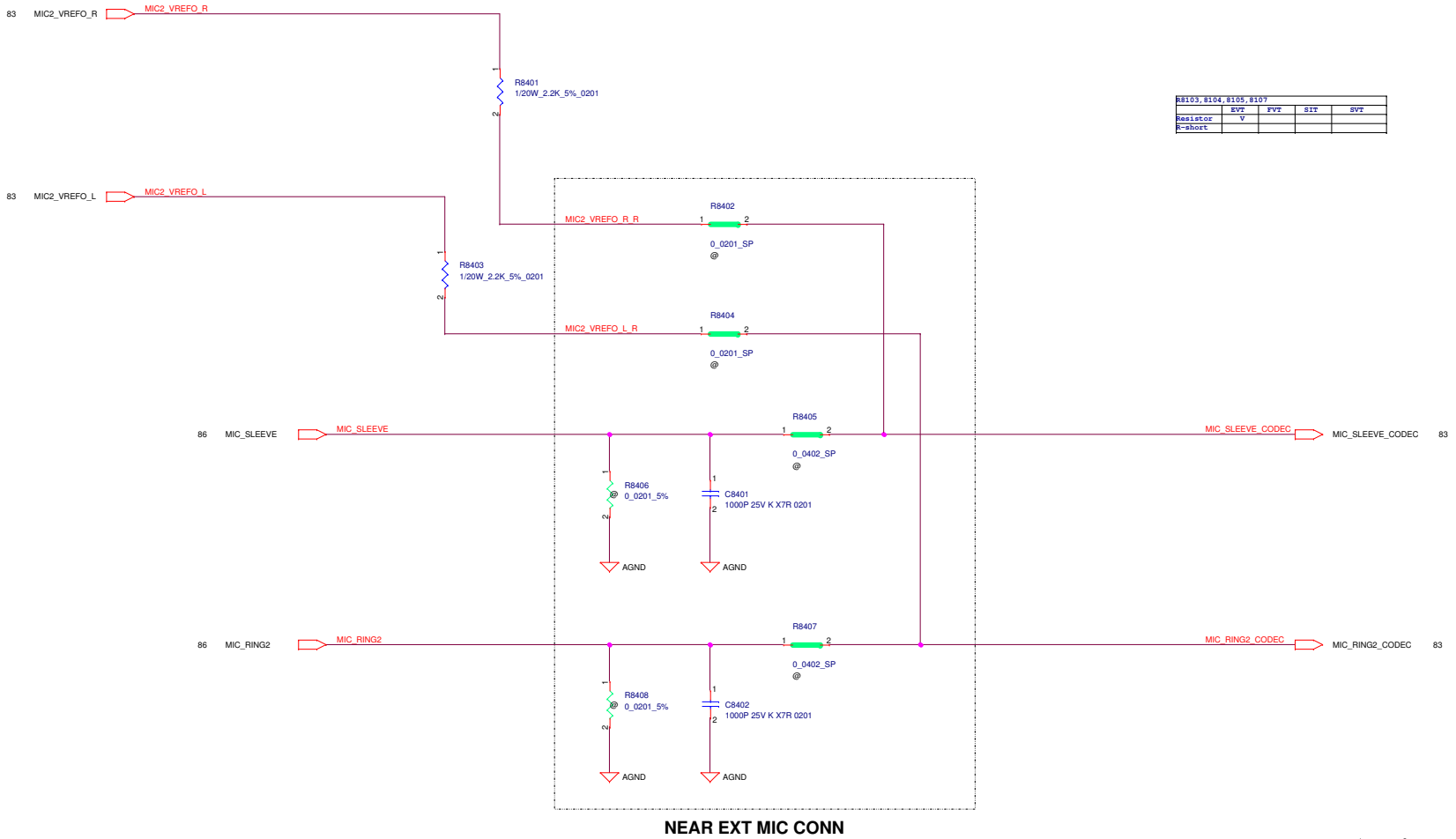
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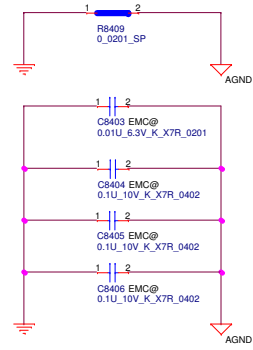
(mA)		D0(+1)	D1	D2	D3
DVDD	1.8V	0.00958	0.00851	0.00012	0.00848
DVDD-IO	1.5V	0.0161	0.0161	0.0161	0.0161
AVDD1	5V	1.49	1.559	0.277	0.92
AVDD2	1.8V	14.45	1.126	0.612	0.597
PVDD1/2	5V	0.0001	0.0001	0.0001	0.0001
Power(mW)		33.501894	9.861768	2.511466	5.714514

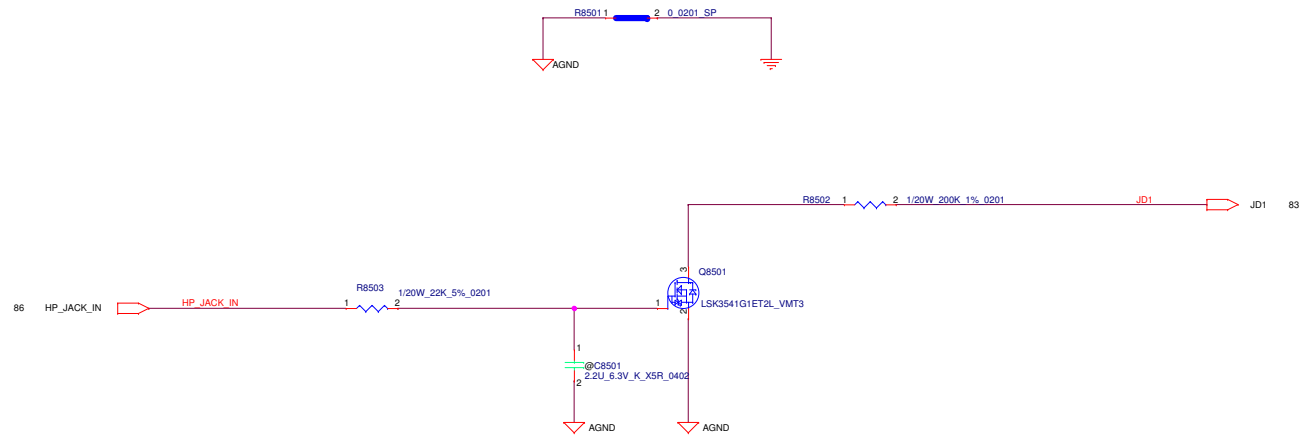
Current Sense Resistor	
R8303	2.0m
R8304	2.0m
R8305	2.0m
R8306	2.0m

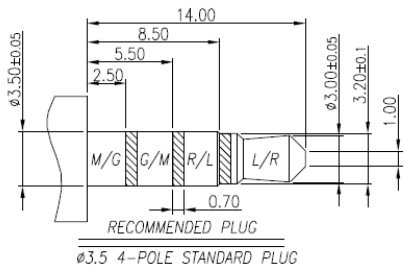
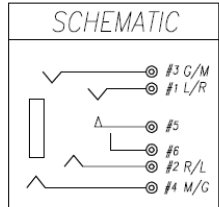




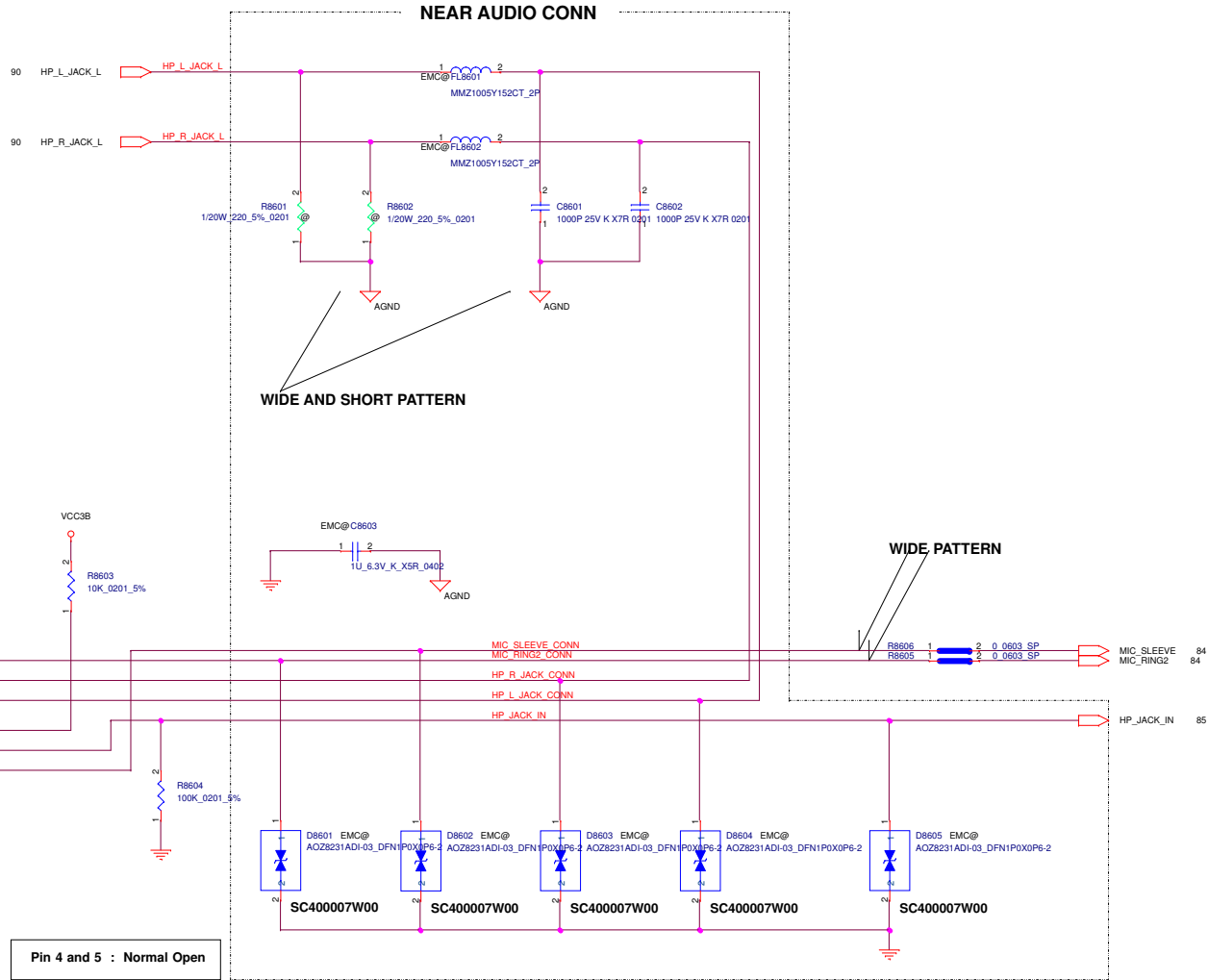
R8103, R104, R105, R107				
Resistor	EV7	FVT	SIT	SVT
R-8000	V			

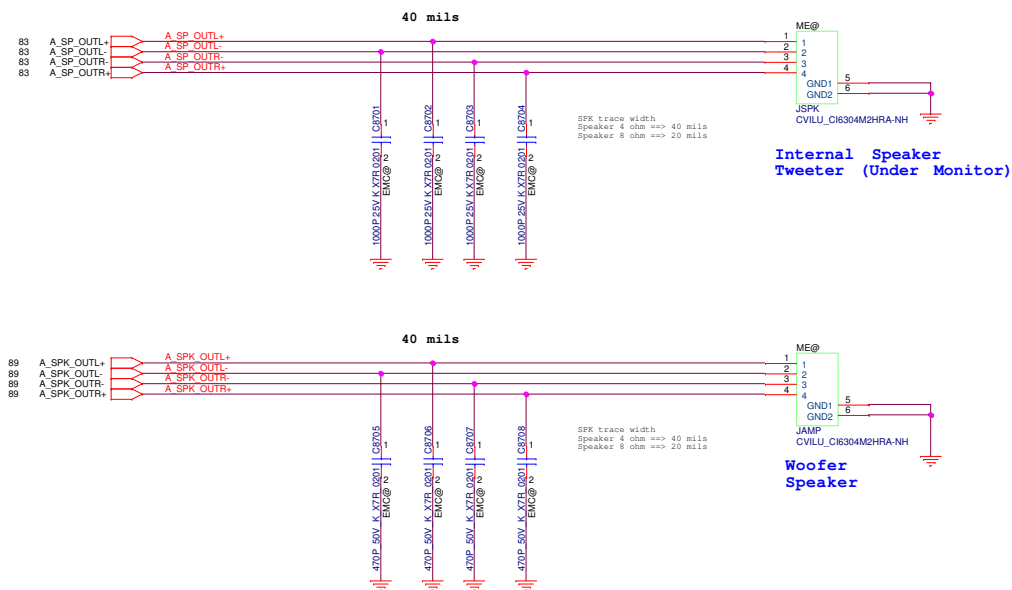






Pin 4 and 5 : Normal Open



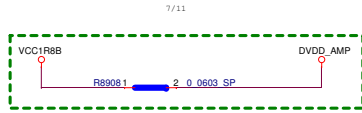


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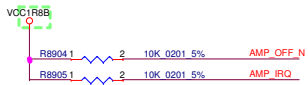
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Size	Title	Rev									
C	Audio(6/8)	2.0									
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83,95,99 VCC1R8B VCC1R8B
DVDD_AMP DVDD_AMP
94,102,103,105,106,108,109,116 VSYS15 VSYS15
VSYS15_AMP VSYS15_AMP

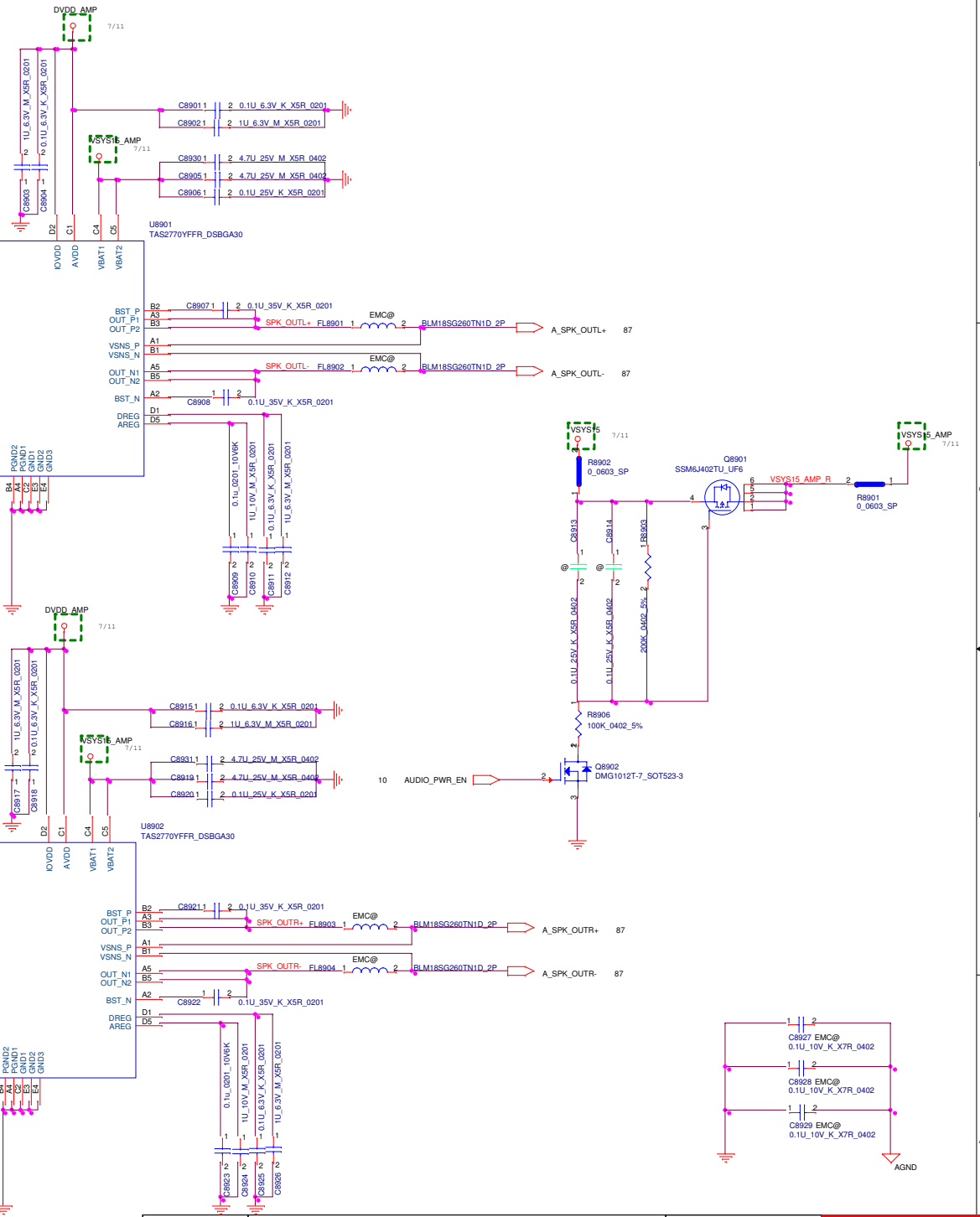
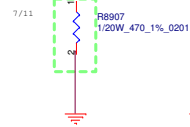
Current Sense Resistor	
R8901	10m
R8908	20m



83,89 I2S_AMP_OUT I2S_AMP_OUT
83,89 I2S_AMP_IN I2S_AMP_IN
83,89 I2S_BCLK I2S_BCLK
83,89 I2S_LRCK I2S_LRCK
83,89 I2C_CLK_AUDIO I2C_CLK_AUDIO
83,89 I2C_DATA_AUDIO I2C_DATA_AUDIO
83,89 AMP_OFF_N AMP_OFF_N
AMP_IRQ AMP_IRQ



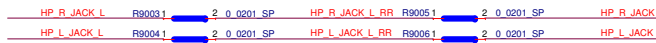
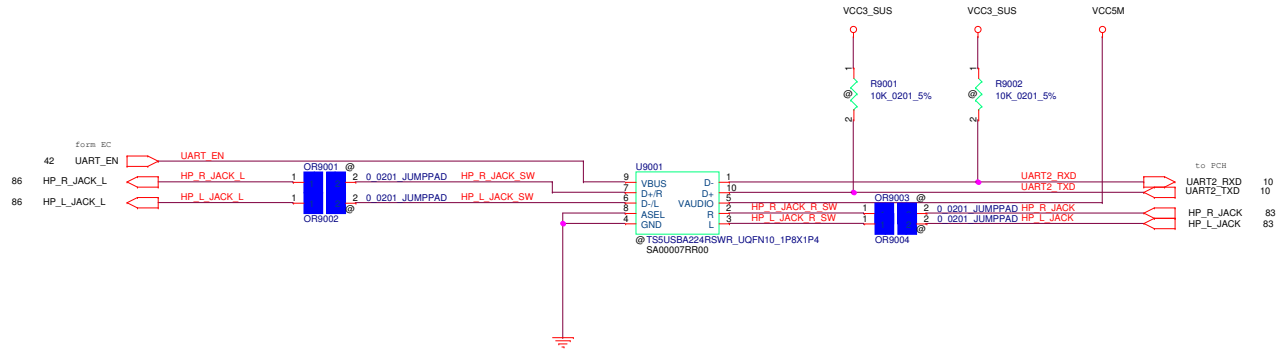
83,89 I2S_AMP_OUT I2S_AMP_OUT
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83,89 I2S_BCLK I2S_BCLK
83,89 I2S_LRCK I2S_LRCK
83,89 I2C_CLK_AUDIO I2C_CLK_AUDIO
83,89 I2C_DATA_AUDIO I2C_DATA_AUDIO
83,89 AMP_OFF_N AMP_OFF_N
AMP_IRQ AMP_IRQ



5,9,10,12,15,18,21,22,42,59,69,72,96,99,108,109 VCC3_SUS
55,59,67,69,99,103,116,123 VCC5M

TABLE:


Mode	Audio	UART
UART_EN	L	H



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Issued Date	2019/06/11	Deciphered Date	2019/06/11	C950						
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Size	Title	Rev								
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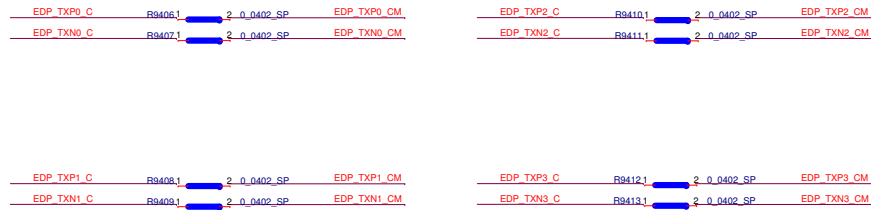
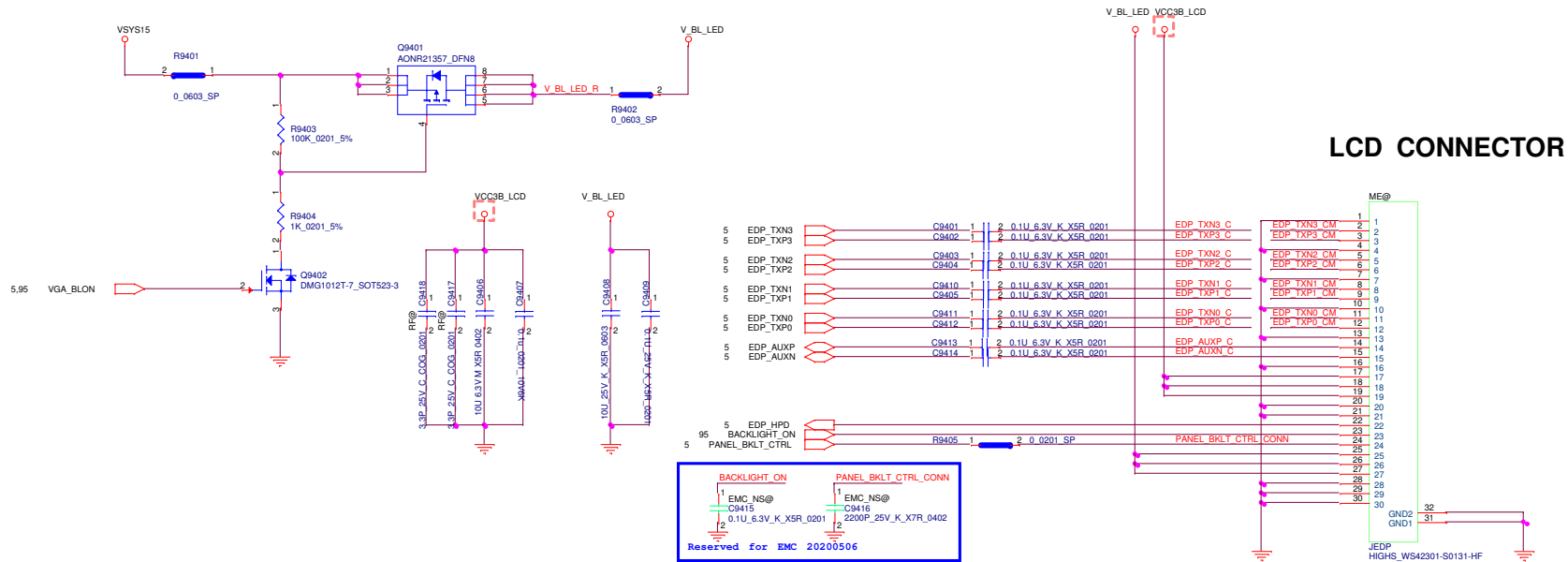
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83,89,95,99 VCC1R8B
 5,99,123 VCC3B_LCD
 89,102,103,105,106,108,109,116 VSYS15
 V_BL_LED

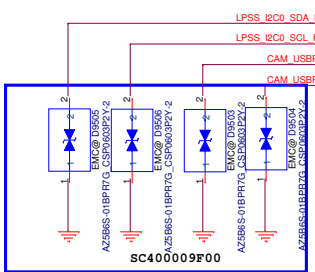
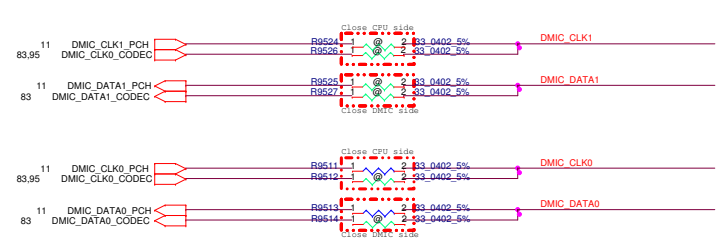
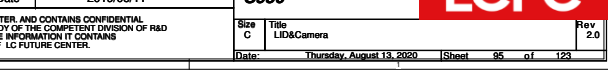
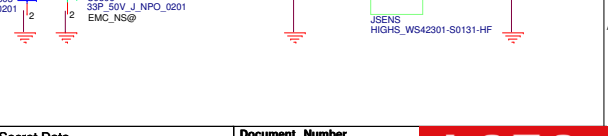
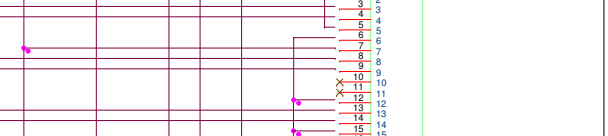
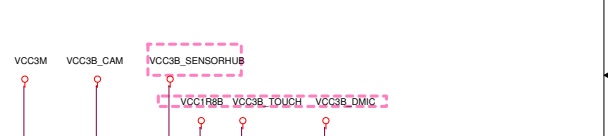
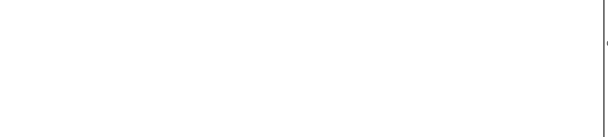
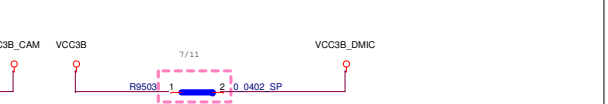
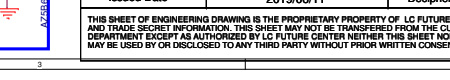
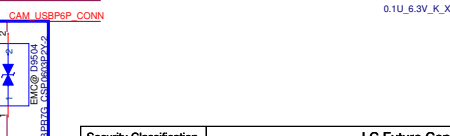
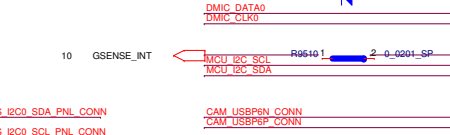
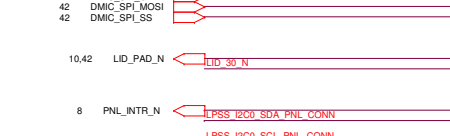
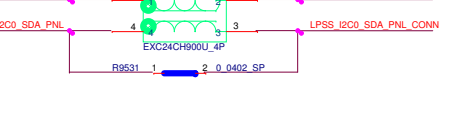
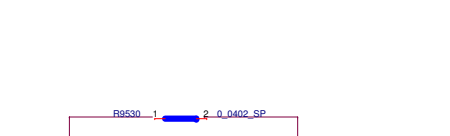
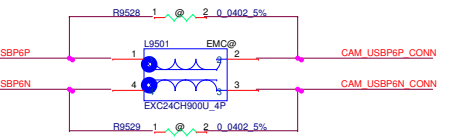
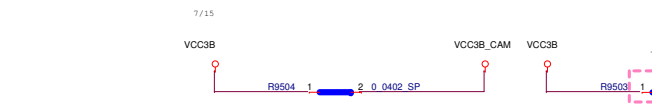
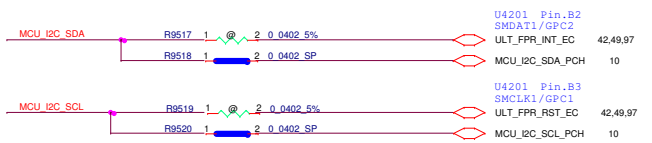
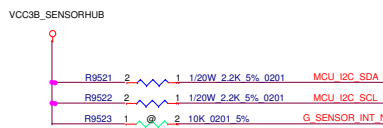
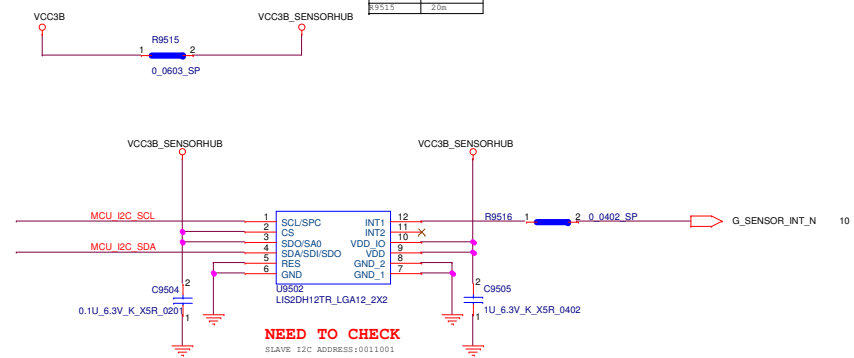
Current Sense Resistor
 R9402 25m

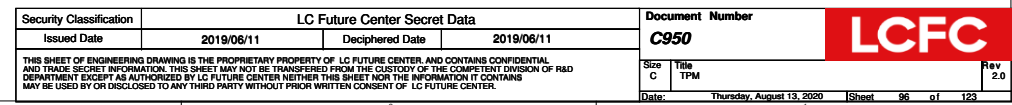
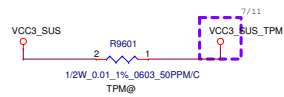


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VCC3B
VCC3B_SENSORHUB
VCC3B_DMIC
VCC3M
VCC3B
VCC3M_FAN
VCC5M_FAN
VCC5B
VCC5B

Current Sense Resistor	
R9503	10m
R9504	10m
R9515	20m

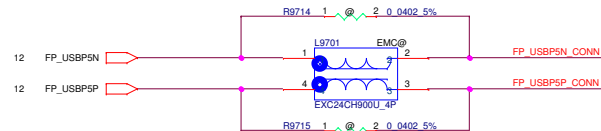
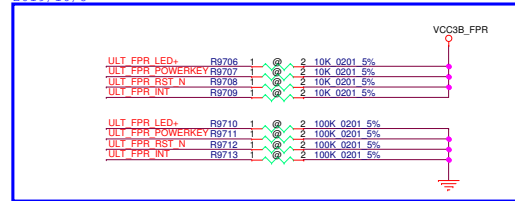




8,9,10,15,21,42,46,49,54,56,69,70,72,86,95,99,106,108,123

VCC3B

VCC3B_FPR

Current Sense Resistor
R9701 10mULTRASONIC FPR
2019/9/26ULTRASONIC FPR PU/PD
Need to verify
2019/10/8

3.2.2 Pin Assignment

PIN ¹⁾	PIN Name ²⁾	Type ³⁾	Function Description ⁴⁾
1 ⁴⁾	LED+ ⁴⁾	Output ⁴⁾	External Led Control signal. Reserved. ⁴⁾
2 ⁴⁾	POWERKEY+ ⁴⁾	Output ⁴⁾	The power supply block Support. Reserved. ⁴⁾
3 ⁴⁾	RESETN ⁴⁾	Input ⁴⁾	MCU Reset Signal, active low. Reserved. ⁴⁾
4 ⁴⁾	INT ⁴⁾	Input ⁴⁾	Interrupt Signal from EC. Reserved. ⁴⁾
5 ⁴⁾	GND ⁴⁾	Ground ⁴⁾	Connect to Ground. ⁴⁾
6 ⁴⁾	USB_DP ⁴⁾	Differential Signal ⁴⁾	Universal Serial Bus D+(USB). ⁴⁾
7 ⁴⁾	USB_DM ⁴⁾	Differential Signal ⁴⁾	Universal Serial Bus D-(USB). ⁴⁾
8 ⁴⁾	D3V3 ⁴⁾	Power ⁴⁾	Power Supply 3.3V (from 3.0 to 3.6V). ⁴⁾

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		2019/06/11

Document Number
C950

LCFC

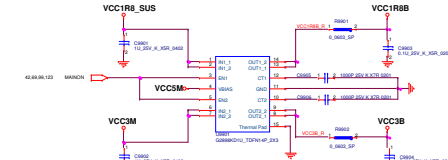
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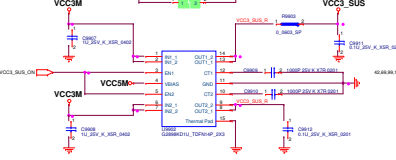
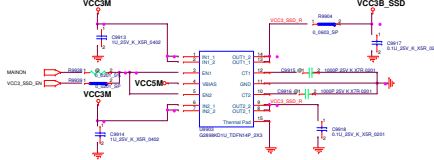
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Size	Title	Rev								
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Date: Thursday, August 13, 2020				Sheet 88 of 123						

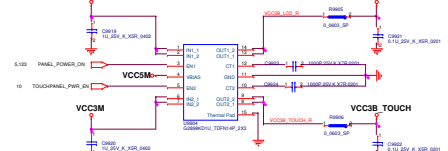
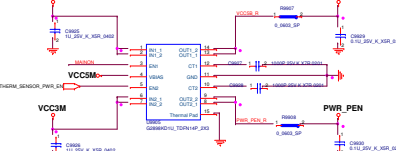
CCIRSB & VCC3B



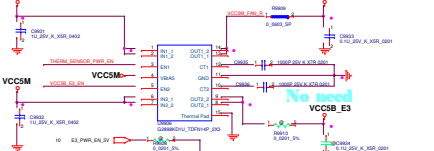
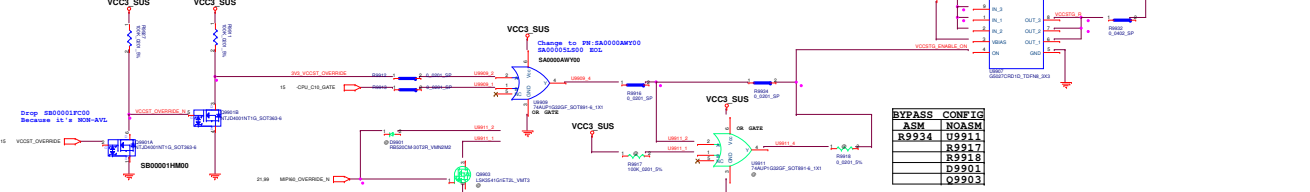
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**VCC3_SSD**

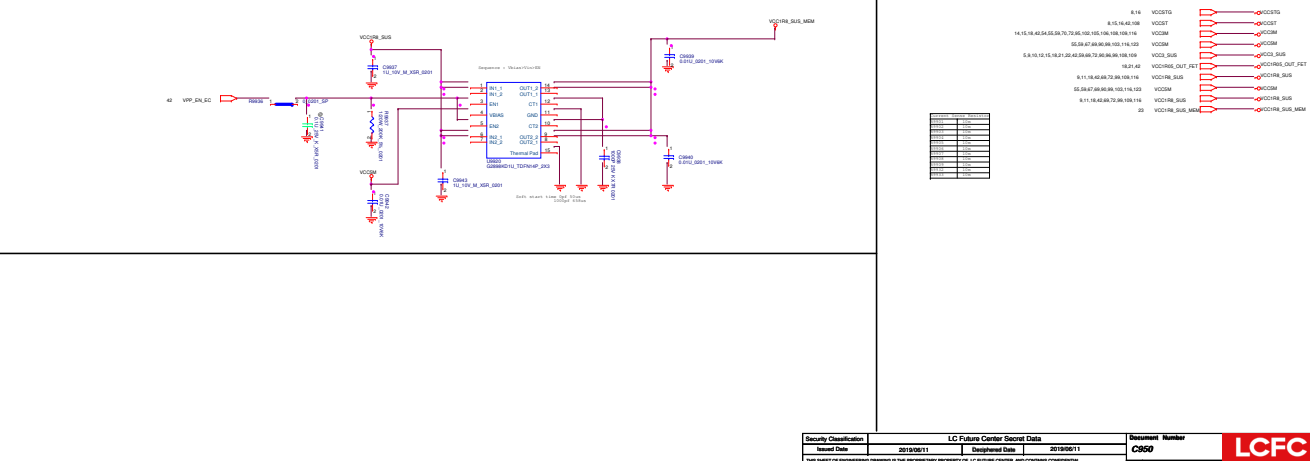
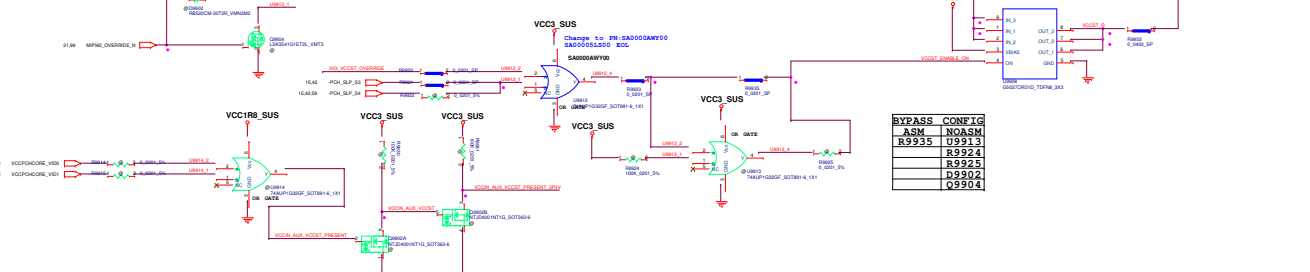
CC3LCD & CC3_TOUCH

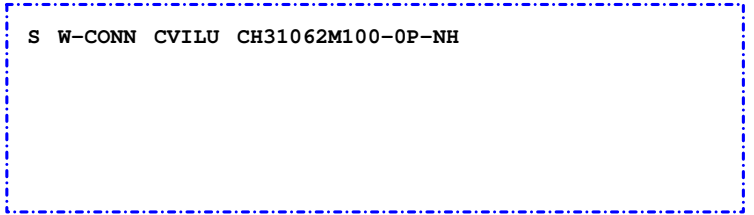
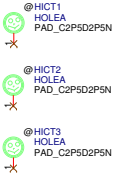
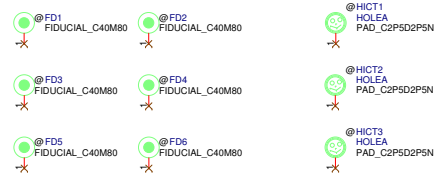
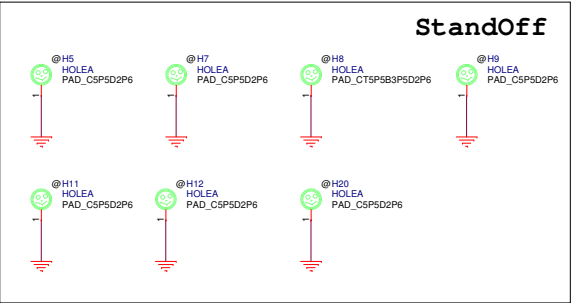
CC5B &
WR_PEN

VCC5M_FAN & VCC5B_E3

**CCSTG**

CCST





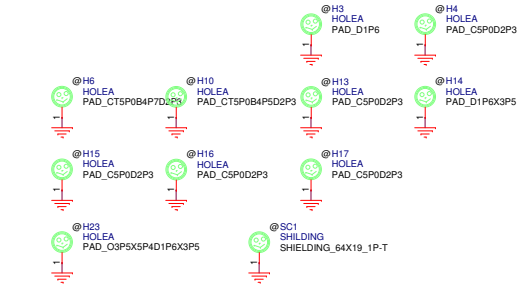
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R1603 10m	R1807 20m	R2309 20m	R4203 10m	R4501 10m	R4601 10m
R1604 10m	R1808 20m	R2309 1m	R4203 10m		
R1611 10m	R1809 20m		R4297 10m		
	R1810 10m				
	R1811 20m				
	R1811 10m				

Current Sense Resistor	Current Sense Resistor	Current Sense Resistor	Current Sense Resistor	Current Sense Resistor	Current Sense Resistor
R5901 1m	R5901 10m	R5901 10m	R5919 10m	R5919 10m	R5919 10m

Current Sense Resistor	Current Sense Resistor	Current Sense Resistor	Current Sense Resistor	Current Sense Resistor	Current Sense Resistor
R9301 20m	R9301 10m	R9402 20m	R9503 10m	R9601 10m	R9701 10m
R9303 20m	R9308 20m		R9504 10m		
R9304 20m			R9513 20m		
R9305 20m					
R9306 20m					

Current Sense Resistor	
R9901 10m	
R9902 10m	
R9903 10m	
R9904 10m	
R9905 10m	
R9906 10m	
R9907 10m	
R9908 10m	
R9909 10m	
R9912 10m	
R9913 10m	

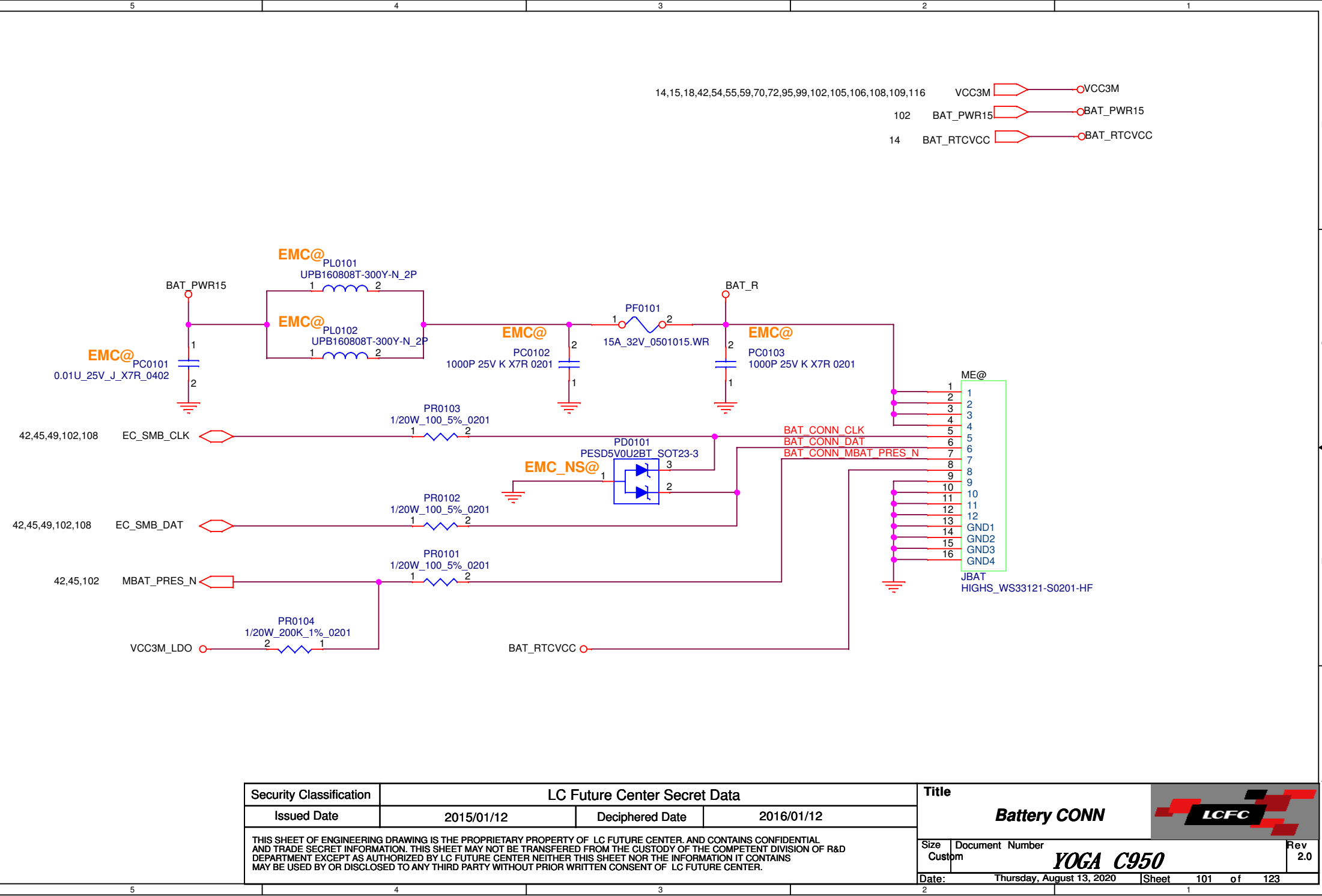
Elastomer Socket

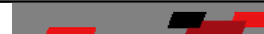


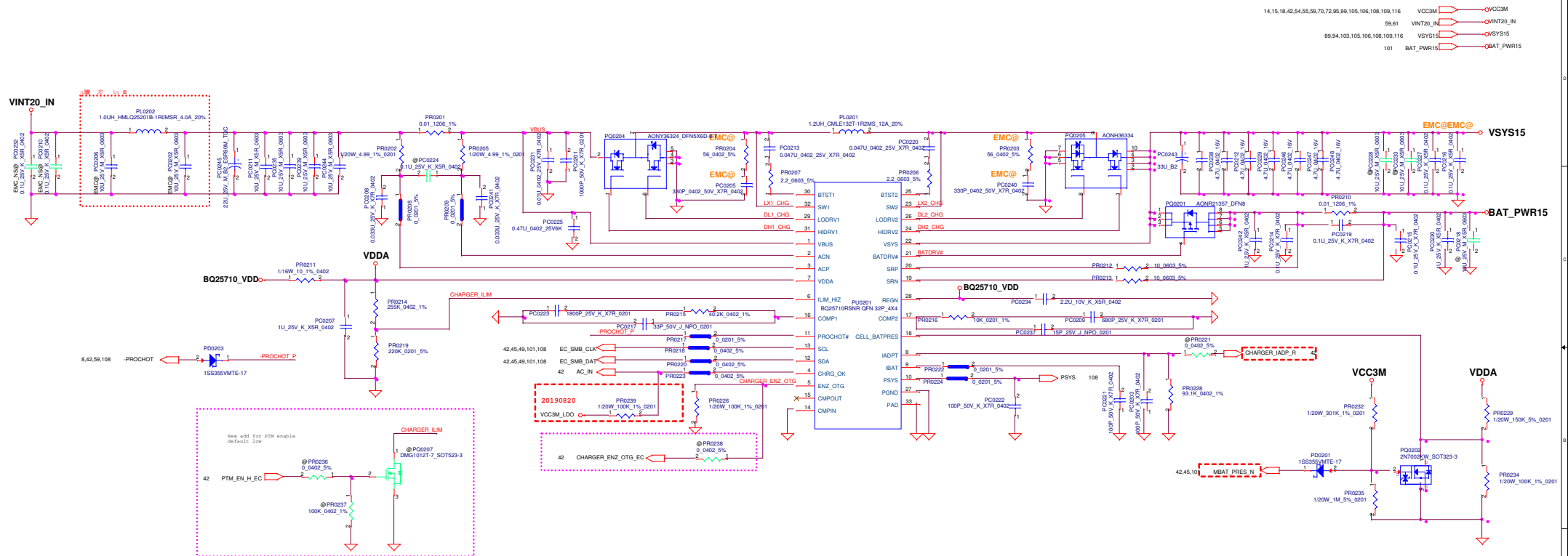
ON BOARD MEMORY

PCB SVT Change to DAZ




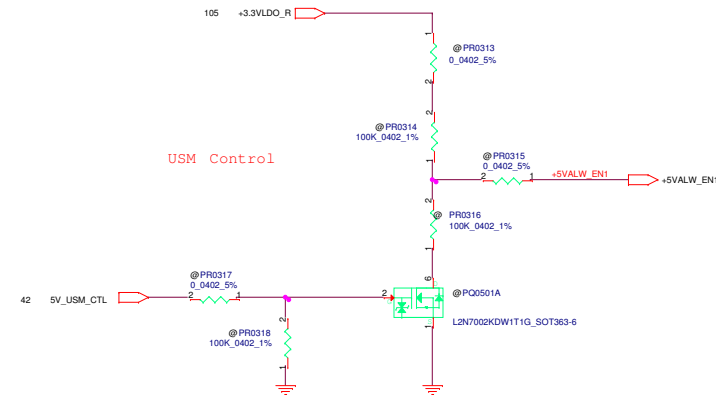
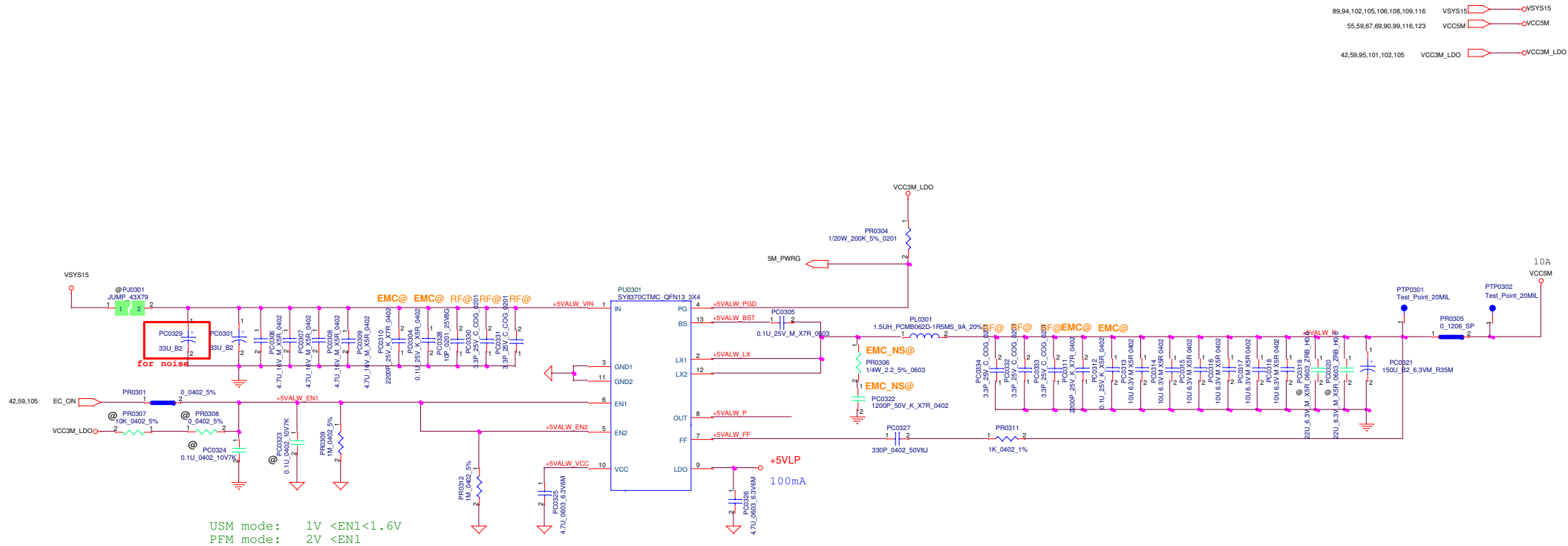


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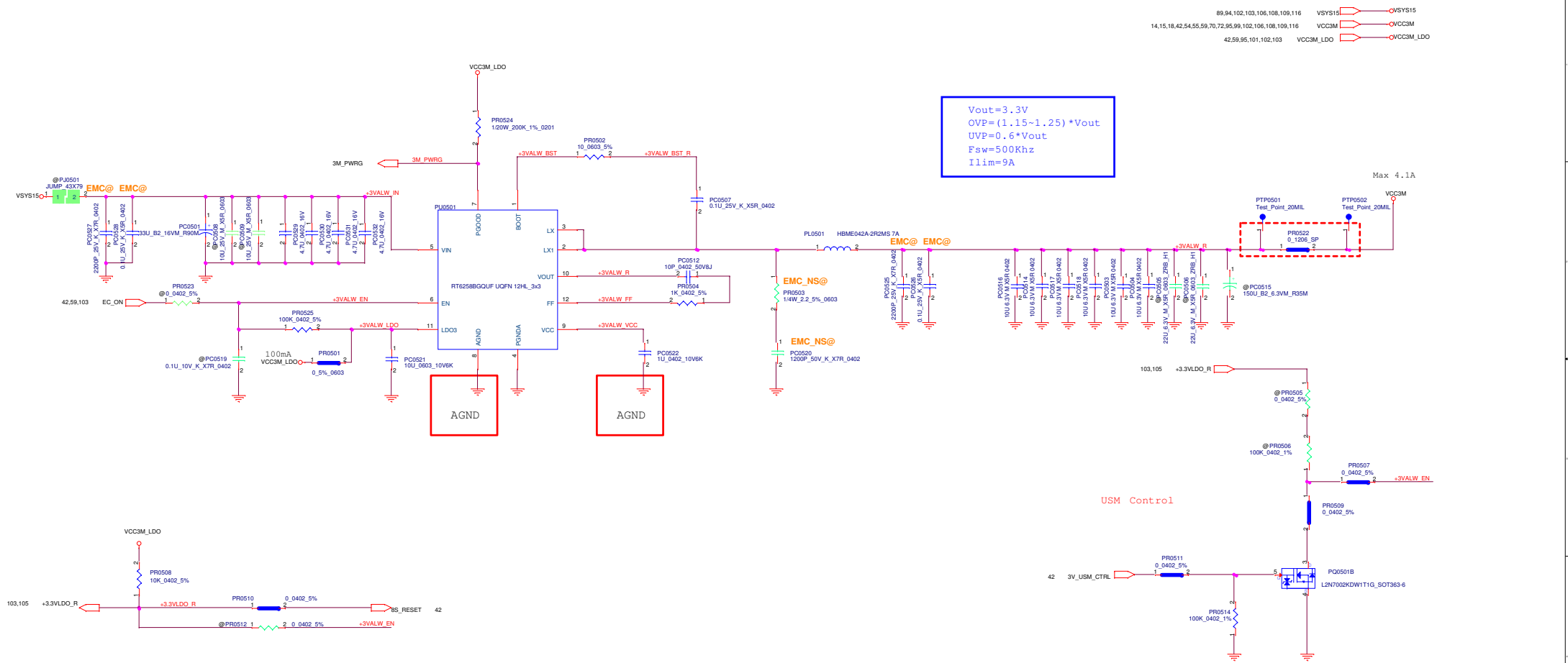
New add for OTG function
Default low
High to enable OTG

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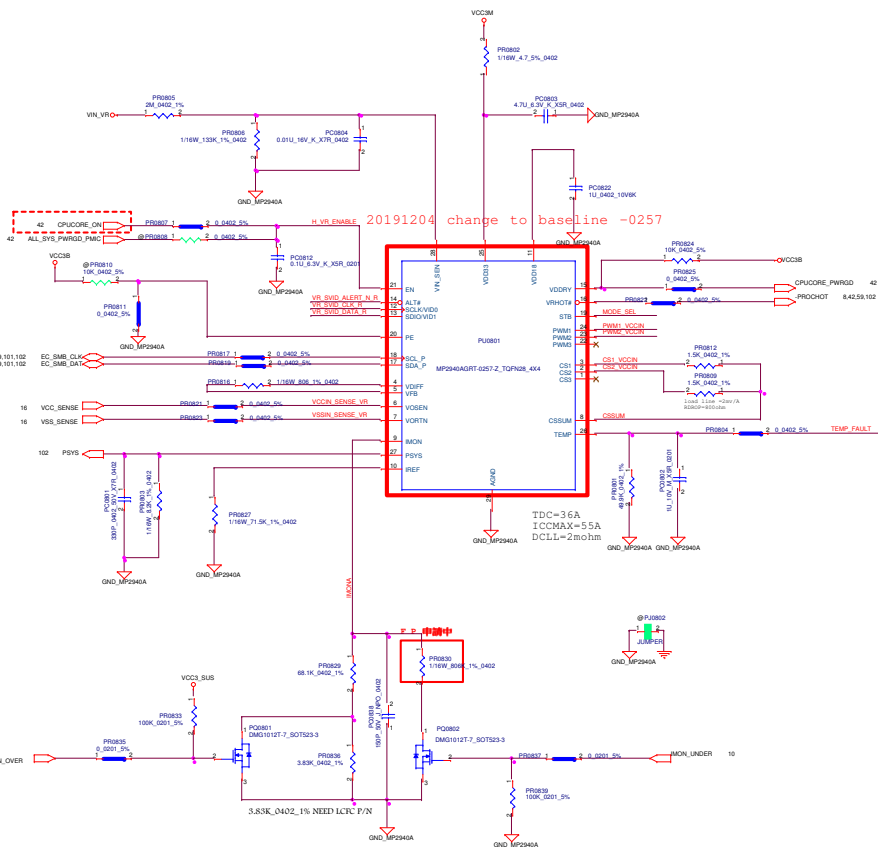
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					Date:	Thursday, August 13, 2020	Sheet 104 of 120



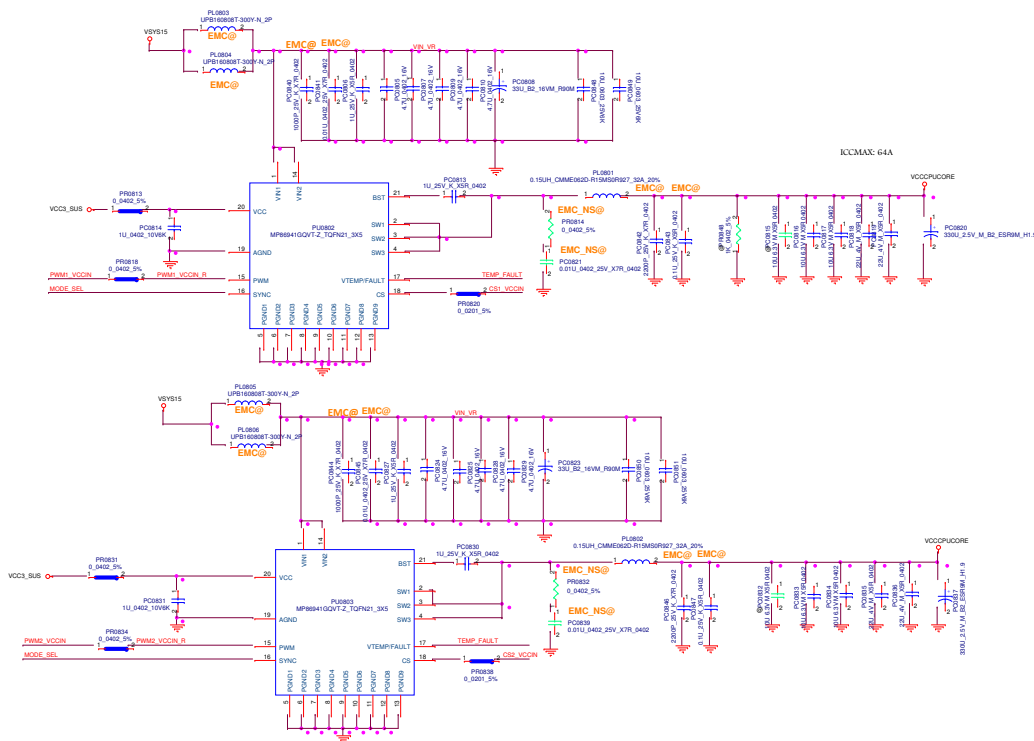
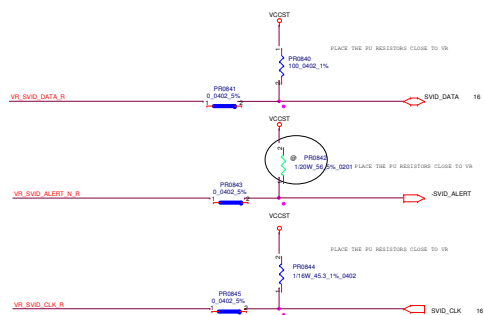
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			Date:	Thursday, August 13, 2020	Sheet 108 of 123

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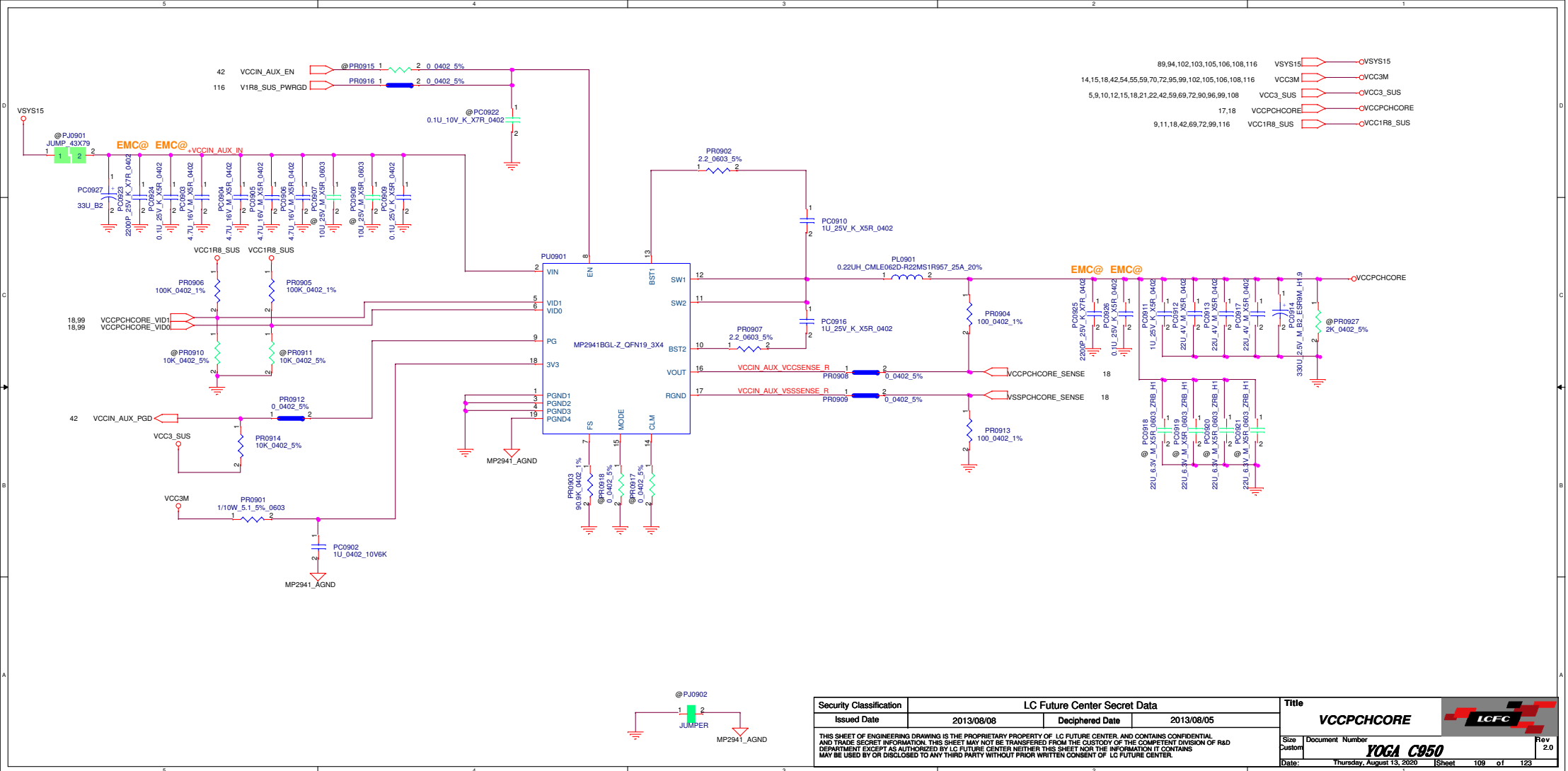
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1. Normal (Default) : IMON_OVER = 1 and IMON_UNDER = 0
2. Performance Mode : IMON_OVER = 1 and IMON_UNDER = 1
3. Moderate Mode : IMON_OVER = 0 and IMON_UNDER = 0




8.9, 10, 15, 21, 42, 45, 54, 56, 69, 70, 72, 86, 95, 97, 99, 106, 125	VDDA	QVDDA
14, 15, 18, 42, 54, 55, 56, 70, 72, 86, 95, 97, 99, 106, 125	VDDC	QVDDC
5, 8, 10, 12, 15, 18, 21, 22, 42, 55, 69, 72, 86, 95, 97, 99, 106, 125	VDDC	QVDDC
16, 17	VDDC	QVDDC
8, 15, 16, 42, 55	VDDC	QVDDC




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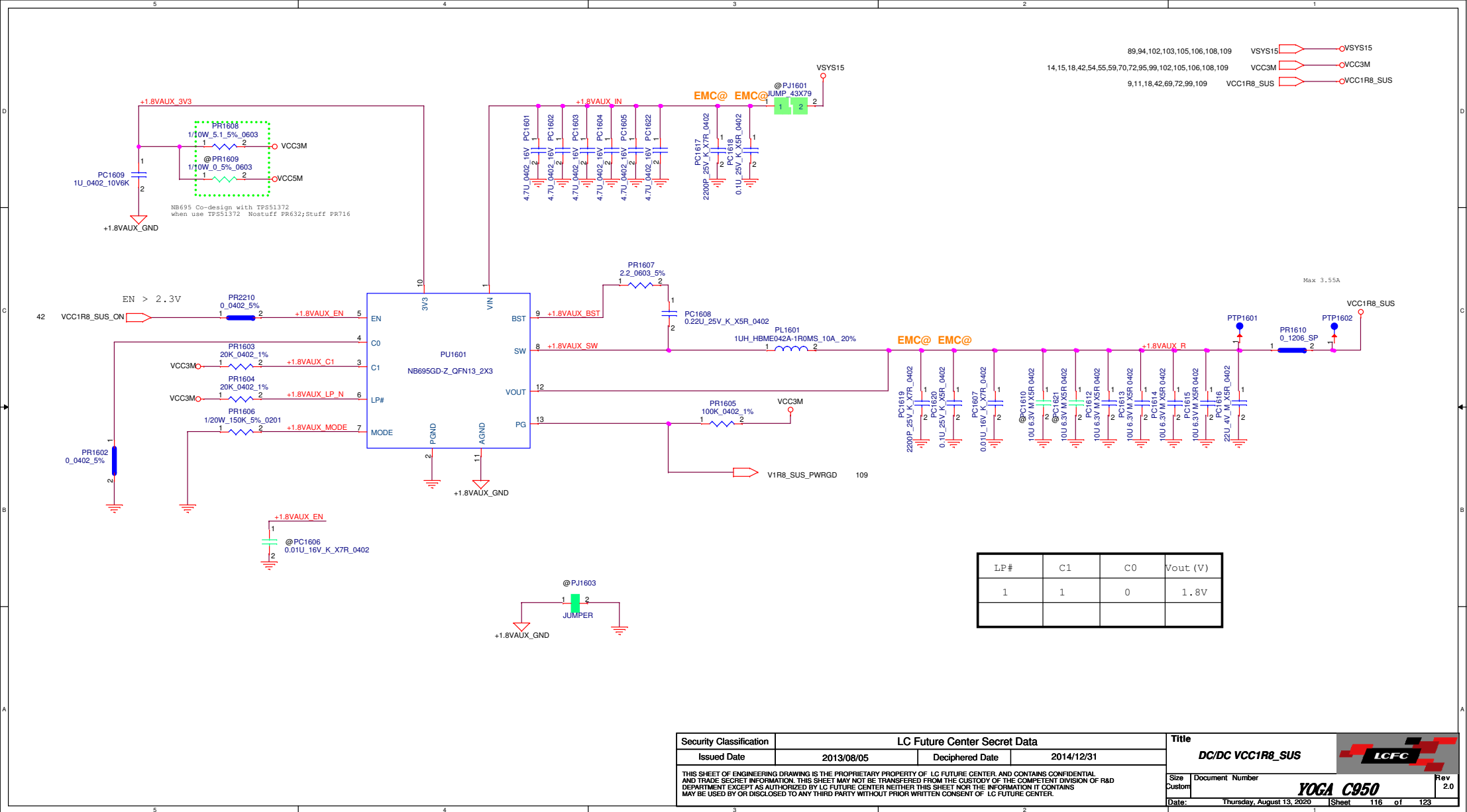
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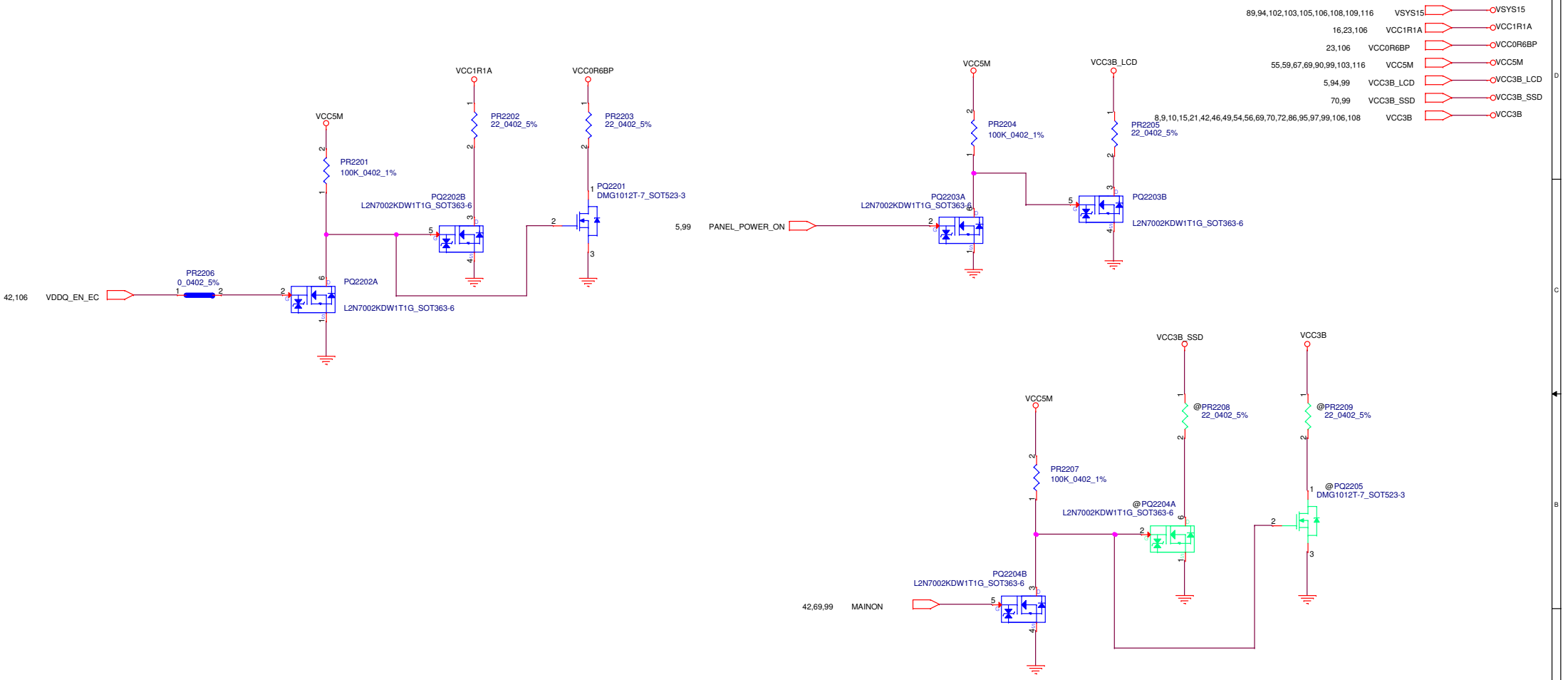
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<table><tr><td>Security Classification</td><td colspan="3">LC Future Center Secret Data</td><td>Title</td></tr><tr><td>Issued Date</td><td>2015/01/12</td><td>Deciphered Date</td><td>2016/01/12</td><td>BLANK</td></tr><tr><td colspan="4">THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.</td><td>Size C Document Number YOGA C950 Rev 2.0</td></tr><tr><td colspan="4"></td><td>Date: Thursday, August 13, 2020 Sheet 121 of 123</td></tr></table>					Security Classification	LC Future Center Secret Data			Title	Issued Date	2015/01/12	Deciphered Date	2016/01/12	BLANK	THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Size C Document Number YOGA C950 Rev 2.0					Date: Thursday, August 13, 2020 Sheet 121 of 123
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- 89,94,102,103,105,106,108,109,116 VSYS15
- 16,23,106 VCC1R1A
- 23,106 VCC0R6BP
- 55,59,67,69,90,99,103,116 VCC5M
- 5,94,99 VCC3B_LCD
- 70,99 VCC3B_SSD
- VCC3B

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